4.11 LOW VOLTAGE LOOP

The circuits described in this section perform the following functions:

(1) Connect the VCA output to the terminals to provide the basic 1V range:
0.09V to 2V

(2) Amplify the VCA output voltages to the instrument's terminals, for the 10V range:
0.9V to 20V

(3) Attenuate basic 1V range voltages to provide the millivolt ranges:
9mV to 200mV on 100mV Range
0.9mV to 20mV on 10mV Range
90μV to 2mV on 1mV Range

(4) Sense the voltages at the output terminals (or at the load in Remote Sense) and scale the signal to the 1V RMS Full-Range level for comparison with the quasi-sinewave.

(5) Provide switching of AC voltage output, Range, Guard and Sense, under the control of signals from the Analog Control Interface.

(6) Detect excess currents in the output circuit, providing a status signal to the CPU via the Analog Control Interface.

(7) Detect excess voltages on the PHi (I+) output line, providing a status signal to the CPU via the Analog Control Interface.

The circuits in this section are located as follows:

Millivolt attenuator and sense circuitry:
— AC Assembly

Power amplification:
— Power Amplifier Assembly.

Output control:
— Output Control Assembly.

Terminals:
— Mother Assembly.
— Terminal Board.

A simplified block diagram of the low voltage loop and routing appears in Fig. 4.11.1.

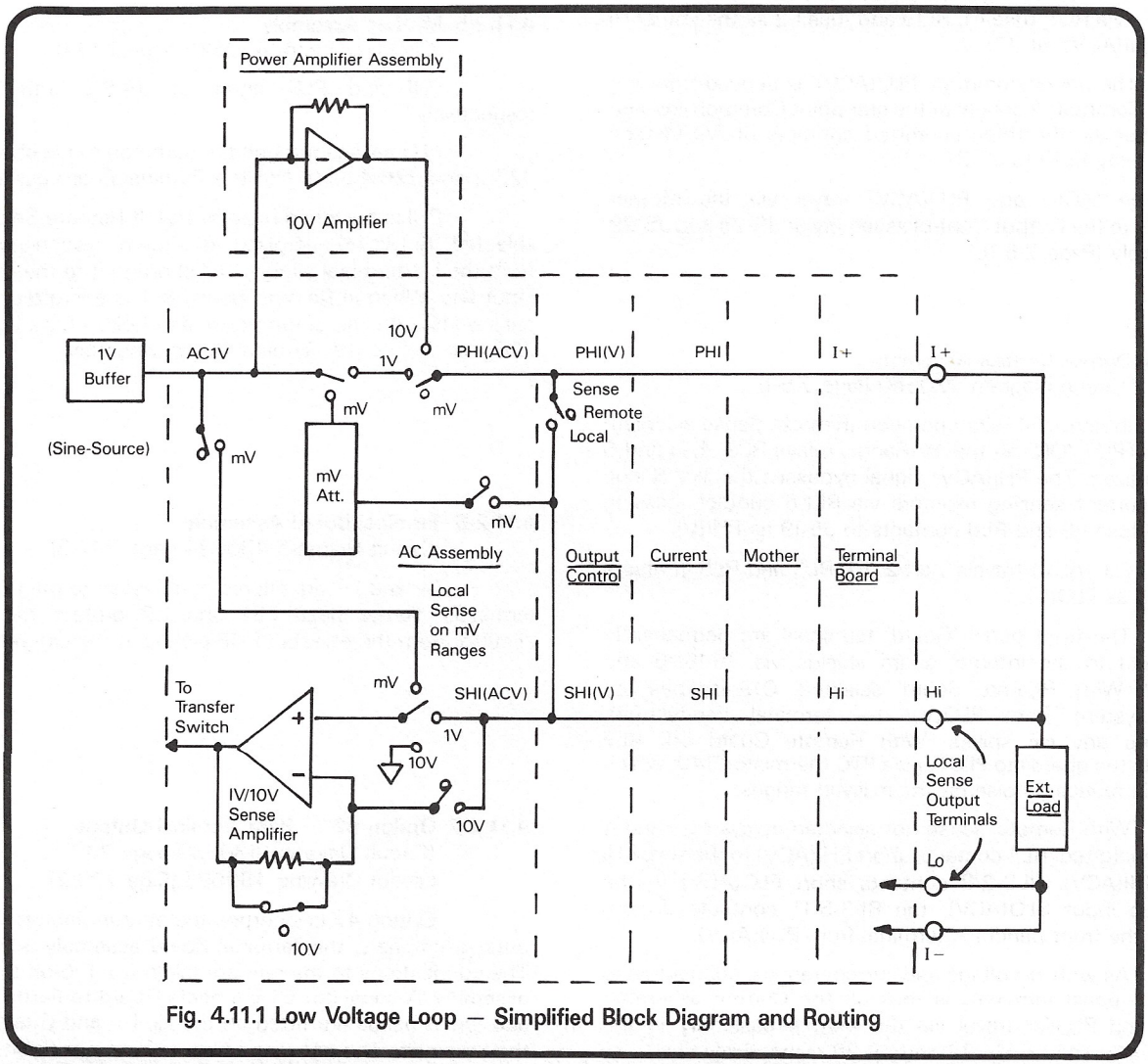


Fig. 4.11.1 Low Voltage Loop — Simplified Block Diagram and Routing

4.11.1 General

This description follows the 1V range path from the VCA buffer to the Sine/Quasi-Sine Comparator (at the input of the transfer switch M16). The 10V and millivolt output and sense conditioning are included.

On the circuit diagrams, the relay contacts are shown in the un-energized condition.

For High Voltage output and sense conditioning see Sections 4.12 and 4.13.

4.11.2 1V Loop — Power Delivery

4.11.2.1 Sine-Source Assembly
(Circuit diagram 430446 Page 7.6-3)

The 1V Buffer (page 7.6-3) is described in Sect 4.10, as part of the output amplitude control circuitry. Its output voltage, signal 'AC 1V' ranging between 0.9V to 2V RMS; is fed out of the Sine-Source assembly on J6-41, via the Mother assembly, and input to the AC assembly on J7-41 (page 7.7-1).

4.11.2.2 AC Assembly
(Circuit diagram 430447 Page 7,7-1)

With the 1V Range selected, relays RL7 (1V) and RL19 ($\overline{1kV}$) are closed, and relays RL4, 5, 6, 17, 18 and 20 are open. So the AC 1V signal is passed directly out of the AC assembly, via RL7, fuse F1, RL19 and fuse F2 as the Power-Hi signal 'PHI(ACV)' at J7-27.

The power common 'PLO(ACV)' is derived from the in-guard Common-2 supply at the star-point Common-2B, and passed out via the three energized contacts of AC Voltage selector relay RL10 to J7-31.

PHI(ACV) and PLO(ACV) travel via the Mother assembly to the Output Control assembly at J5-25 and J5-29 respectively (Page 7.5-1).

4.11.2.3 Output Control Assembly
(Circuit diagram 430550 Page 7.5-1)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the 1V Range, relays RL3, 4, 5 and 6 are energized. The PHI(ACV) signal bypasses the 1kV Range output current sensing resistors via RL1-6 contact, passing through fuse F3 and RL6 contacts to J5-19 as PHI(V).

PLO(ACV) travels via F2, F1, RL3 and RL5 contacts to J5-23 as PLO(V).

The front panel 'Guard' terminals are permanently connected to the internal guard shields via J5-15/16 and J5-11/12. With 'Remote Guard' selected, C19 isolates the guard system from PLO(V) (I− terminal connection), bypassing any HF spikes. With Remote Guard off, RL7 connects the guards to PLO(V) via PTC thermistor R40, which assists in reducing noise on the millivolt ranges.

With Remote Sense not selected, relays RL3 and 4 are un-energized. RL4 contacts short PHI(ACV) to the sense Hi input SHI(ACV). RL3-2/8 contacts short PLO(ACV) to the sense Lo input SLO(ACV); the RL3-5/11 contacts disconnecting the front panel I− terminal from PLO(ACV).

As with all voltage and current ranges, connection to the front panel terminals is through the Current assembly. PHI(V) and PLO(V) travel via the Mother assembly to the Current assembly at J8-25 and J8-29 respectively.

4.11.2.4 Current Assembly
(Circuit Diagram 430555 page 7.8-1)

With any Voltage Range selected, relays RL8 and 9 are un-energized as shown. RL23 is energized; connecting PHI(V) to J8-8/9 as 'PHI' and PLO(V) to J8-16/17 as 'PLO'.

PHI and PLO then pass into the Mother assembly.

If the Current option is not fitted, a Link PCB (part No. 410182) is fitted in its place. This shorts:
J8-25 — PHI(ACV) to J8-8/9 — PHI,
J8-29 — PLO(ACV) to J8-16/17 — PLO.
The connections do not involve relay switching.

4.11.2.5 Mother Assembly
(Circuit Diagram 430532 page 7.16-1)

PHI and PLO enter at J8-8/9 and J8-16/17 respectively.

PLO passes through the common mode choke L1 via J23-3 and J26-4 as 'I−' to the Terminal Board assembly.

PHI is switched by relay RL1. If Remote Sense is not selected, RL1 is un-energized as shown; disconnecting PHI from the I+ terminal circuit, and shorting it to the sense SHI input line. When in Remote Sense RL1 is energized, and PHI passes through the common mode choke L1 via J23-1 and J26-1 as 'I+' to the Terminal Board assembly.

4.11.2.6 Terminal Board Assembly
(Circuit Diagram 430634 page 7.17-3)

I+ and I− are filtered and passed to the front panel terminals. Ferrite bead FB1 and C2 protect the internal circuitry from the effects of HF pickup in the external circuit.

4.11.2.7 Option 42 — Rear Terminal Output
(Circuit Diagram 430530 page 7.17-1
Layout Drawing 480603 page 7.19-2)

Option 42 is incorporated at manufacture. With rear output terminals, the Terminal Board assembly is not fitted. The connections to the rear are taken fro J26 on the Mother assembly. A capacitor C1 connects Guard to Earth (Ground), and ferrite beads are fitted on the Hi, I+ and Guard leads at the terminals. The mV range filter relay is not fitted.

4.11.3.1 Terminal Board Assembly
(Circuit Diagram 430634 page 7.17-3)

For the users with Option 42 — Rear Output, the circuitry at the terminals is changed. Refer to sect. 4.11.2.7.

If Remote Sense is selected, the front panel sense terminals Hi and Lo are connected externally to I+ and I− respectively, at the load.

The sensed voltage is filtered by FB2 and C3 to remove external HF pickup. This rejection is augmented by C1 for the millivolt ranges and for 'AC Zero' output selection. A signal ('R−', 'R+'), originating as 'TERM FILTER' in the Reference Divider, operates relay RL1 on the millivolt ranges. (Circuit Diagram 430535 page 7.4-4).

The filtered sense voltage is fed into the Mother assembly between J26-2 (HI) and J26-5 (LO). (No external sensing is provided for the millivolt ranges. See para 4.11.5 and Fig. 4.11.1 for the local sensing arrangement.)

4.11.3.2 Mother Assembly
(Circuit Diagram 430532 page 7.16-1)

LO passes through the common mode choke and directly to the Current assembly at J8-18 as SLO.

HI also passes through the choke and enters the Current assembly as SHI at J8-10. However, if Remote Sense is not selected, it is shorted to PHI by relay RL1. RL1 is energized from the REM SENSE + and − lines from the Output Control assembly.

4.11.3.3 Current Assembly
(Circuit Diagram 430555 page 7.8-1)

With any Voltage Range selected, relays RL8 and 9 are un-energized as shown. RL23 is energized; connecting SHI into the Mother assembly as 'SHI(V)' via J8-26, and SLO via J8-30 as 'SLO(V)'.

If the Current option is not fitted, the Link PCB shorts:

J8-10 — SHI to J8-26 — SHI(V),
J8-18 — SLO to J8-30 — SLO(V).

The connections do not involve relay switching.

4.11.3.4 Output Control Assembly
(Circuit Diagram 430550 page 7.5-1)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the 1V Range, relays RL3, 4, 5 and 6 are energized. SHI(V) enters from the Mother assembly at J5-20 and is passed directly through RL6 contacts (OUTPUT ON) and out via J5-26 as SHI(ACV).

SLO(V) travels via RL5 contacts (OUTPUT ON) to J5-30 as SLO(ACV).

With Remote Sense not selected, relays RL3 and 4 are un-energized. RL4 contacts short SHI (ACV) to the power Hi output PHI(ACV). RL3-2/8 contacts short SLO(ACV) to the power Lo output PLO(ACV).

SHI(ACV) and SLO(ACV) travel via the Mother assembly to the AC assembly at J7-28 and J7-32 respectively (Page 7.7-1).

4.11.3.5 AC Assembly
(Circuit Diagram 430447 page 7.7-1)

SLO(ACV) passes via the energized contact of the AC Voltage selector relay RL10, to be referred to the Sense Amplifier common 'SIG LO'.

With the IV Range selected, relay RL19 ($\overline{1kV}$) contacts are closed, so SHI(ACV) appears at RL19-11 as 'SENSE HI' (Refer to the circuit diagram on page 7.7-2).

With the 1V Range selected, relay RL8 (1V) is energized, thus SENSE HI is applied to the non-inverting input of the Sense Amplifier via R126. RL14 is un-energized as shown, so the inverting input via R115 is referred to SIG LO.

RL3 ($\overline{100V + 1kV}$) is energized, connecting the Sense Amplifier output to the Sine/Quasi-Sine comparator transfer switch M16-11 (page 7.7-3).

A description of the Sense Amplifier appears in Section 4.11.4.

4.11.4 1V Sense Amplifier

(Circuit Diagram 430447 page 7.7-2)

The same amplifier is used on the 10V, 1V, 100mV, 10mV and 1mV Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

On the 1V and millvolt ranges it is connected as a voltage-follower, sensing always being carried out at the 1V level. The 1V range sense signal originates at the load in Remote Sense, or in the Output Control assembly in local sense. For the millivolt ranges the 'AC1V' drive to the millivolt attenuators is sensed directly (see sect. 4.11.5).

On the 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

Separate arrangements are made for attenuation and scaling on the 100V and 1kV ranges. These are described in Section 4.13.

4.11.4.1 General

A discrete amplifier is used to provide the required slew rate up to 1MHz, all time constants being set well above 1MHz, with the first pole above 5MHz. It is configured into its follower circuit by relay switching.

Relays RL8, RL12 and RL3 are all energized on the 1V range. Relays RL11, RL13, RL14, RL15 and RL16 remain un-energized as shown in the diagram.

Dual JFET Q41 is a unity gain buffer in totem pole configuration. It drives the input protection diodes D37-D40, D44-D47, and the screen of Q40 inverting input; also driving the bootstrap buffer Q46. The total input capacitance is thus reduced to 1 – 1.5pF.

The differential input amplifier, Dual FET Q40, has low input capacitance, and low input current. Q36 provides constant-current drive to Q40 and the bootstrapped followers Q38/Q39. R107 permits initial DC input-offset cancellation. The stage gain is low.

Emitter-followers Q34 and Q35 buffer the high-impedance low-gain FET stage, driving a differential signal into the high gain voltage amplifier Q29/Q30. This arrangement has the advantage of placing all the gain in one stage. The single-ended drive to Q31 output stage is taken from Q30 collector.

Q24 and Q25 form a current mirror to equallize the collector currents of Q29 and Q30, preventing signal injection into the sense amplifier power rails.

L6 and L7 isolate the amplifier power rails from the 15V supply at HF. C50 is the main frequency-response compensation capacitor, providing smooth roll-off, with unity gain at around 5MHz.

On the IV Range, the output from Q31 is returned at low impedance, as 100% negative feedback to the amplifier input, via the closed contacts of RL12-8/14.

4.11.5 Millivolt Loop

(Circuit Diagram 430447 pages 4.7-1 and 4.7-2)

The basic 1V loop is extended by inserting a switched, passive, attenuator network. The switching circuit connects the selected millivolt output via RL19-11/8 directly to the SHI(ACV) line, not 'PHI'. Thus only the two front panel Sense Hi and Lo terminals are used to connect to the load.

The software forces Remote Sense OFF in the millivolt ranges. Except for a series resistor (R154) on the 1mV range, the AC1V signal is connected directly to the input of the Sense Amplifier at RL8-13. The Amplifier circuit remains permanently in its non-inverting 1V configuration for all three millivolt ranges, so local sensing is carried out at 1V range levels.

Thus the output value at the terminals depends on both the calibrated value of the AC1V signal and the division ratio of the attenuator. In addition to the 1V range calibration, each millivolt range is also 'Autocalibrated' separately (refer to Section 1).

4.11.5.1 Millivolt Attenuators

(Fig. 4.11.2)

The AC1V signal is diverted from its 1V range route by the un-energized contacts of relay RL7. It is applied to the attenuator network via RL7-11.

The fixed chain (formed by R120 in series with the parellel combination of R112B and R110) is permanently connected between RL7-11 and the Common-2 star-point. Three levels of attenuation are achieved by switching R112A and R118. Relay RL5 is eneregized for the 10mV range only, RL6 for the 100mV range. The three arrangements are shown in Fig. 4.11.2.

On the 1mV range, the series resistor R154 is connected between RL7-11 and the Sense Amplifier input via RL11-5, but it is shorted on the 10mV and 100mV ranges by the closed contacts of RL5 and RL6 respectively.

Relay RL4 is energized on all millivolt ranges. The attenuator output is passed out to the SHI(ACV) line via RL4-8/9 and RL19-11/8. Capacitor C89 defines the specified bandwidth, filtering noise at HF.

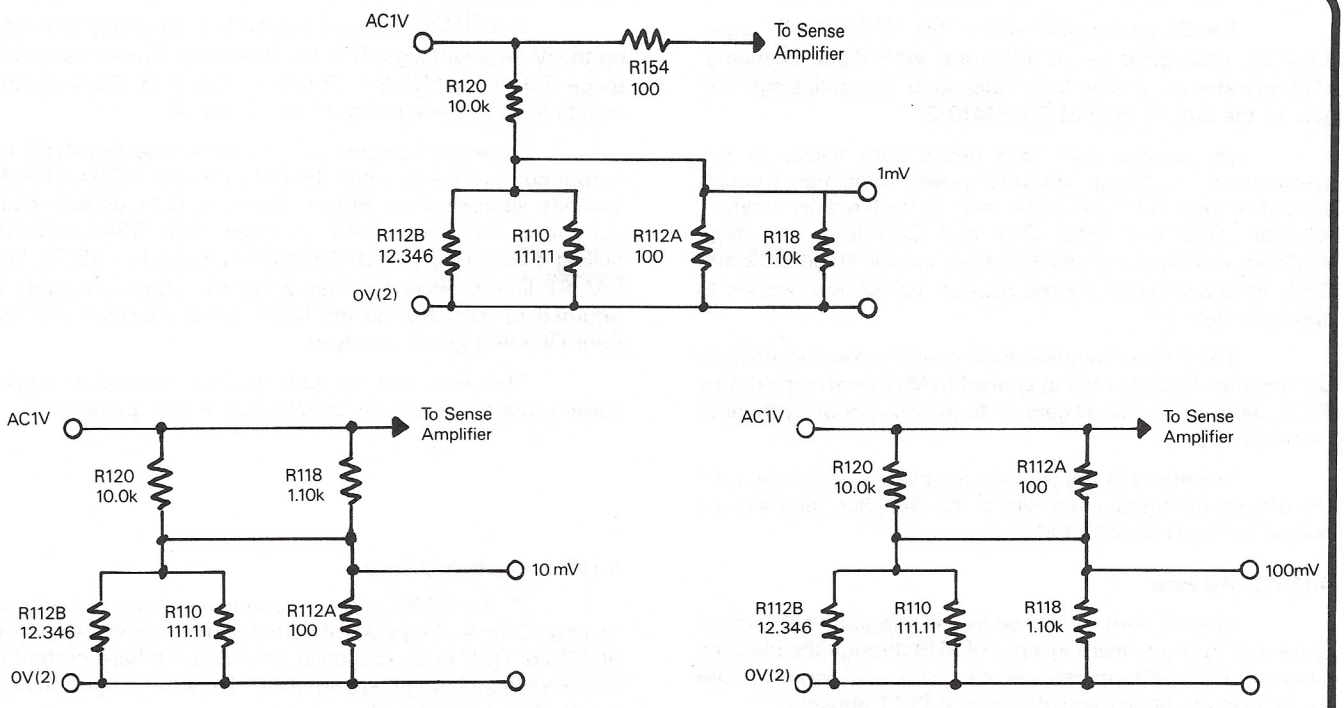


FIG. 4.11.2 MILLIVOLT ATTENUATORS
(Resistance in Ohms)

4.11.6 10V Loop

(Circuit Diagrams: 430446 page 7.6-3,
430450 page 7.9-1 and 430447 page 7.7-1)

As noted in section 4.11.2, the 1V Buffer is part of the power delivery system for all ranges. On the 10V range its output (AC1V) passes via J6-41 from the Sine-Source assembly and into the Power Amplifier assembly (PA) at J9-36.

The AC1V signal is amplified by a factor of 10 in the inverting 10V Power Amplifier, whose output is switched onto the 'AC 10V + 100V' line. This 10V range signal returns to the AC assembly at relay contacts RL17-13/4. It passes through RL19-2/5 to the PHI(ACV) line at J7-27.

The 10V range outputs then follow the same route (to and from the output terminals) as the 1V signals. Whether in Remote Sense or not, the sensed voltages return via the SHI(ACV) line to the same Sense Amplifier used for 1V range signals.

With 10V range selected, the sense amplifier has an inverting gain of 0.1, returning the signal to the 1V levels required by the Sine/Quasi-Sine comparator.

4.11.7 10V Power Amplifier

(Circuit Diagram 430450 page 7.9-2)

The AC1V signal enters the PA assembly at J9-36, passing to the input of the 10V Power Amplifier via relays RL4-9/13 and RL3-9/13. It is referred to common 2B by developing a voltage across R124. The amplifier is best regarded as having separate DC and AC paths.

4.11.7.1 DC Path

The DC path is blocked by C56; M17 is the DC input amplifier, connected as an integrator with diode clamping. M19 operates as an inverter in open loop, so applies high DC gain to the output from M17 on M19-2.

The output from M19 drives both halves of the symmetrical, inverting, discrete power amplifier through current-limiters Q21 and Q24, and is buffered by emitter-followers Q22 and Q23. Q27 and Q29 form a voltage amplifier, driving the complementary output stage Q32 and Q33. R119 and R120 set the gain of the discrete stages to approximately 4.5.

The forward amplification contains three inversions, DC negative feedback being applied to M17 inverting input by R122, defining an overall gain of 10 in conjunction with input resistor R123.

The effect of the DC path is to sense and correct the DC offsets throughout the whole AC amplifier, referring the output to Common-2A at M17-3.

4.11.7.2 AC Path

The AC path is blocked by the integrator M17, but is applied to the non-inverting input of M19 through the blocking capacitor C56. M19 operates in open loop, applying its output to the discrete power amplifier (see 4.11.7.1 above).

The amplifier AC gain is also set to 10 by R122 and R123, the circuit time constants being selected to allow overall instrument output operation over the full frequency range of 10Hz to 1MHz.

4.11.7.3 Power Supplies

M17 and M19 are supplied from ± 15V common-2A rails, the discrete amplifier from the ± 38V supply, which is used solely for this purpose.

4.11.7.4 Overload Detection

The $\overline{\text{LIM ST}}$ line, connected to D74 anode, is pulled up to 0V (in-guard logic-1) in the Reference Divider assembly (page 7.4-4) by AN2-9/1 (1MOhm). The Error OL message results from this line being driven to logic-Ø.

Overload detector Q31 reaches Vbe threshold on output current peaks, when the RMS value in R139 and R141 exceeds approximately 80mA. Similarly, Q34 detects peak currents in R147 and R149. In either case, Q34 conducts, pulling diodes D71 and D74 cathodes down to −15.7V. The $\overline{\text{LIM ST}}$ line is driven to logic-Ø, so the status message is returned to the CPU via the SSDA serial interface, and the Error OL message is displayed.

This does not preclude further increase in output current, but the accuracy specification is not guaranteed.

4.11.7.5 Overload Limiting

If the RMS output current increases to approximately 100mA, the peaks of current cause the Vbe threshold of Q28 or Q30 to be exceeded, shunting the base current of the corresponding voltage amplifier. Thus the output drive to the final stage is limited.

4.11.7.6 Output Protection

The output current passes through the combination of R144 and L8. At low frequencies the inductor provides a low output impedance, whereas at high frequencies the resistor stabilizes the amplifier when driving capacitive loads.

4.11.8 10V Sense Amplifier

(Circuit Diagram 430447 page 7.7-2)

The same amplifier is used on the 10V, 1V, 100mV, 10mV and 1mV Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

On the 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

On the 1V and millivolt ranges it is connected as a voltage-follower. The millivolt ranges are simply the 1V range after passive attenuation, sensing always being carried out at the 1V level.

Separate arrangements are made for attenuation and scaling oin the 100V and 1kV ranges. These are described in Section 4.13.

4.11.8.1 General

A general description of the Sense Amplifier is given in Section 4.11.4.1 for the 1V range.

4.11.8.2 10V Range Configuration

On the 10V Range, relays RL14 and RL3 are both energized. Relays RL8, RL11, RL12, RL13, RL15 and RL16 remain un-energized as shown in the diagram.

The 'SENSE HI' signal is routed to the inverting input of the amplifier through the closed contacts of RL14 and resistor R115. With relays RL8 and RL11 not energized, the non-inverting input is referred to SIG LO.

The output from Q31 is returned via R121 as negative feedback to the amplifier input, the contacts of RL12-8/14 being open.

Thus the circuit is configured as an inverting amplifier, resistors R115 and R121 scaling the sense signal down by a factor of 10. Extensive screening is employed at the amplifier's virtual ground, bootstrapped by buffers Q46 and Q41 to follow the virtual-common potential. This reduces the input capacitance, which is further compensated by feedback capacitor C60.

4.11.9 AC Assembly Logic and Relay Drives
(Circuit Diagrams 430447 page 7.7-5)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = −15V, logic-1 = 0V.

The signals enter the AC assembly via J7 from the Mother assembly.

M28 and M29 are inverting, open-collector Darlington drivers. The relay-drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (−15V) on those not required. A selected driver operates its relay by pulling its output to −14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J7-53 is pulsed to logic-Ø for 50ms. Q19 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD (IG)}}$ pulse has ended Q19 turns off, and they are held on by the -12.6V between −1.4V at the cathode of D20 and −14V at the selected driver output. This method reduces the heat, generated locally by energized relay solenoids, in the relay contacts.

FETs Q42 and Q43 damp the coil of RL12 and RL13; diodes D59 and D60 isolate the parts of the printed circuit to these relays which are sensitive to power-common breakthrough, when they are deselected. D55 and D56 are overswing diodes.

4.11.9.1 Range Switching
(Page 7.7-5)

Range control data is input as a 3-bit code on AC RØ, AC R1 and AC R2 lines. The bit-pattern is decoded to '1 of 8' by M25, to energize the correct relays for the selected range.

In the 4200 only eight of the M25 'Q' outputs are connected. The resulting variants are listed in Table 4.11.1 against range selections.

Function Note |1|	Range	Range Code $ACR_{2-Ø}$ ACR_2 ACR_1 $ACR_Ø$			M25 Output at Logic-1 'Q'	Pin	Relays Energized [* = Energized] 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AC Volts	1000V	0	0	0	Q0	3	*								*			*			*				*
	100V	0	0	1	Q1	14	*								*					*		*		*	
$\overline{\text{AC FNCT}}$ at Logic-Ø,	10V	0	1	0	Q2	2	*	*							*				*			*		*	
	1V	0	1	1	Q3	15	*	*				*	*		*		*							*	
$\overline{\text{IFNCT}}$ at Logic-1)	100mV	1	0	0	Q4	1	*	*	*		*				*	*	*							*	
	10mV	1	0	1	Q5	6	*	*	*	*					*	*	*							*	
	1mV	1	1	0	Q6	7	*	*							*	*	*							*	
	Any	1	1	1	Q7	4	*	*							*								*	*	
AC Current $\overline{\text{AC FNCT}}$ at Logic-1,	100μA, 1A	0	1	1	Q3	15	*	*				*	*	*			*							*	
$\overline{\text{IFNCT}}$ at Logic-Ø)	1mA, 10mA, 100mA	0	1	0	Q2	2	*	*						*					*			*		*	

Note |1| With the 4200 operating normally: either $\overline{\text{AC FNCT}}$ or $\overline{\text{I FNCT}}$, but not both, will be at logic-Ø; unless SAFEtY message is displayed.

TABLE 4.11.1 AC ASSEMBLY SWITCHING LOGIC

4.11.9.2 $\overline{\text{AC FNCT}}$ and I $\overline{\text{FNCT}}$ Logic
(Page 7.7-5)

In addition ot its primary function of controlling Voltage range switching, the AC assembly logic also needs to respond to Current range selections if Option 30 is fitted; because the AC voltage reference for the Current assembly is generated by the Voltage circuitry. For this purpose the two signals $\overline{\text{AC FNCT}}$ and I $\overline{\text{FNCT}}$ are used.

$\overline{\text{AC FNCT}}$ is at logic-Ø only when Voltage output is selected, holding M25-11 'D' input at logic-1, and energizing relays RL2 and RL10. The bit-patterns controlling the voltage range switching are shown on Table 4.11.1.

$\overline{\text{I FNCT}}$ is at logic-Ø only when Current output is selected, holding M25-11 'D' input at logic-1, and energizing relays RL2 and RL9. This connects the ACI REF lines (J7-69 to J7-72) to the ACV lines. The 10V range circuitry is used on the 100mA, 10mA and 1mA Current ranges, but the 1V range circuitry is used on the 100μA and 1A ranges. The bit-patterns controlling the current range switching are also shown on TAble 4.11.1.

The signals $\overline{\text{AC FNCT}}$ and I $\overline{\text{FNCT}}$ are never at logic-Ø at the same time in normal operation. The only time they are at logic-1 together is when all outputs from the Control Data latches in the Reference Divider are 'Tristated'.

4.11.9.3 'AC Zero'

For zero output, the lines from the voltage generators to the I+ and I− terminals are disconnected by deselection of the ranges, and a hard short is placed across the output lines by RL18.

The AC $R_{2-Ø}$ code is '1,1,1'. This sets M25-4 to logic-1 (energizing relays RL18) and all other M25 range outputs to logic-Ø (the resultant bit-pattern is shown in Table 4.11.1). Thus all ranges are deselected, but relays RL2 (ACV and ACI), RL3 (Low Voltage Output), RL10 (ACV) and RL19 ($\overline{\text{1kV}}$) remain energized). Relay RL18 connects the star-point of Common-2B (PLO) to the PHI (ACV) line.

4.11.9.4 'BARK DELAYED'

The 'BARK' signal does not affect the AC assembly relays. However, if the Watchdog is activated, the CPU imposes OUTPUT OFF conditions and forces the Precision DC Reference to ramp down to zero, so the PHI REF voltage also falls to zero.

All outputs from the Control Data latches in the Reference Divider are 'Tristated' by the 'BARK DELAYED' signal. This allows the pull-up resistors (AN4 and AN5) to become effective.

The $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are pulled to logic-1, and the AC $R_{2-Ø}$ code is '1,1,1'. This imposes 'AC Zero' conditions on the analog sircuit, but RL2 and RL10 are also de-energized. So the DC precision reference is disconnected from the quasi-sinewave generator; the Sense and Power Lo lines are disconnected from the sense amplifiers.

4.11.10 Output Control Assembly, Logic and Relay Drives
(Circuit Diagrams 430550 Page 7.5-1)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = −15V, logic-1 =0V.

The signals enter the Output Control assembly via J5 from the Mother assembly.

The five inverters of M3 are open-collector Darlington drivers. The relay-drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (−15V) on those not required. A selected driver operates its relay by pulling its output to −14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J5—104 is pulsed to logic-Ø for 50ms. Q1 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD (IG)}}$ pulse has ended Q1 turns off, and they are held on by the −12.6V between −1.4V at the cathode of D1 and −14V at the selected driver output. This method reduces the heat, generated locally by energized relay solenoids, in the relay contacts.

4.11.10.1 Remote Sense Logic

With Remote Sense selected, the REM SENSE signal is at logic-1. RL3 and RL4 are energized via M1-6 and M3-16 removing the shorts from across the PHI/SHI lines and PLO/SLO lines. Also, RL3-5/11 completes the circuit of PLO to the voltage output relay RL5. With Remote Sense off, RL3 and RL4 are un-energized, and their contacts are as shown (but see 4.11.10.3 below for Current ranges operation).

4.11.10.2 Remote Guard Logic

With Remote Guard selected, the REM GU signal is at logic-1. RL7 is energized via M1-2 and M3-13 disconnecting the internal guards and the Guard terminals from PLO. With Remote Guard not selected, the guards and terminals are connected to PLO as shown.

4.11.10.3 $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ Logic
(Page 7.5-1)

In addition to its primary function of controlling the output switching, the Output Control assembly logic also needs to respond to Current function selection.

If Option 30 is fitted, the outputs from the voltage circuits need to be isolated from the output terminals. Also, because the AC voltage reference for the Current assembly is generated by the Voltage circuitry, the output/sense loop is completed in the AC assembly. Thus the local sense connections between PHI and SHI, and between PLO and SLO, are not required, and could generate noise in the loop. For this purpose the two signals $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are used.

$\overline{\text{AC FNCT}}$ is at logic-Ø only when Voltage output is selected, energizing relays RL5 and RL6 via M4-6 and M3-11, providing the Output is On and the watchdog has not 'barked'. For Current ranges, $\overline{\text{AC FNCT}}$ is at logic-1, so RL5 and RL6 are un-energized as shown, breaking the lines between the voltage circuitry and the output terminals.

$\overline{\text{I FNCT}}$ is at logic-Ø only when Current output is selected, ensuring that relays RL3 and RL4 are energized, even though Remote Sense is not selected on Current ranges. This removes the local sense shorts, as though in Remote Sense.

The signals $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are never at logic-Ø at the same time in normal operation. The only time they are at logic-1 together is when all outputs from the Control Data latches in the Reference Divider are 'Tristated'.

4.11.10.4 'HIGH I LIMIT' and 'AC 1kV RANGE' Logic

The effects of these signals are described in paras 4.11.2.3 and 4.12.7.5.

4.11.11 High Voltage Status Detector
(Circuit Diagram 430550 Page 7.5-2)

In order to provide information to the CPU, so that it can decide whether the High/Low voltage state is as demanded, the voltage level on the PHI(ACV) line is sensed and compared against a reference.

M5 is a dual comparator whose hysteresis is set to ±0.9V by D8/D9, R34/R35 and R37/R36. For as long as the voltage on the PHI(ACV) line remains within approx. ±125V, the division ratio of M7 keeps the input to M5-5/9 within the ±0.9V hysteresis, and M5-12/7 remains at logic-1 (approx. +14V).

Monostable M2 is set to produce a logic-1 at its Q output (M2-7) unless its B input at M2-5 is edge-triggered negatively. In 'Low Voltage State' conditions no trigger is given, so M2-7 remains at logic-1, D4 is reverse-biased, Q2 is cut off and the $\overline{\text{HV ST}}$ line remains at the analog control logic-1 level of 0V.

If the instantaneous PHI(ACV) voltage exceeds the ±125V limits (corresponding to a sinewave RMS of >90V), either M5-7 or M5-12 pulls towards logic-Ø. Current source Q3 permits only 3mA to flow in M5 output circuit, so the voltage input to M2-5 (B trigger) suffers a negative-going trigger edge.

Monostable M2 produces a negative-going pulse of 130ms duration, which forward-biasses D4, Q2 conducts and the $\overline{\text{HV ST}}$ line transmits a logic-Ø pulse of 130ms duration. This is passed to the CPU, via the status register in the reference divider and the serial data interface.

The CPU has to make a decision, as to whether the programmed output voltage and the detected state are compatible. If they are not, the CPU displays 'FAIL 2', switches Output OFF, trips the watchdog and sets 'FAIL 5' display. Refer to section 2.

4.11.12 Overvoltage Detector
(Circuit Diagram 430550 Page 7.5-2)

An absolute limit of 1440V RMS is placed on the operation of the internal output circuitry. In order to give effect to this limit, the voltage level on the PHI(ACV) line is sensed and compared against a reference.

M6 is a dual comparator whose hysteresis is set to ±1.22V by D8 and D9. For as long as the voltage on the PHI(ACV) line is less than 1440V RMS, the division ratios of M7, R26 and R25 keep the input to M6-5/9 within the ±1.22V hysteresis, and M6-12/7 remains at logic-1 (approx. —1V). Q2 is cut off and the LIM DET line remains at the analog control logic-Ø level of —15V, due to D6 being below threshold.

If the instantaneous PHI(ACV) voltage exceeds the 1440V RMS limits (corresponding to a sinewave peak of ±2025V), either M6-7 or M6-12 pulls towards logic-Ø. Q4 conducts, forward biassing D6 and lifting the LIM DET line to approx. —1V (analog control logic-1 level). This is passed to the $\overline{\text{LIM ST}}$ logic circuitry.

Refer to Section 4.12 for subsequent action. The event is reported to the CPU via the $\overline{\text{LIM ST}}$ logic, resulting in an 'Error OL' display,

4.12 HIGH VOLTAGE POWER DELIVERY
(Circuit Diagram 430450 page 7.9-1)

The AC1V signal, generated by the 1V Buffer in the Sine-Source assembly, enters the Power Amplifier as for the 10V range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 100V range, the signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of 100, the amplifier output being delivered via the 'AC 10V+100V' line to the PHI (ACV) line on the AC assembly.

For the 1000V range the DC Reference is scaled in software, so that the AC1V signal Full Scale value represents 1100V output. The signal is routed through extra stages of amplification before being applied to the 100V Amplifier, whose output now drives one of two 1:6 step-up transformers (LF or HF). The power-amplifier gain on the 1000V range is controlled by feedback from the transformer secondary, into the input of the 1000V Error Amplifier. The 'AC 1kV' line transfers the transformer output to the AC assembly, where it is switched onto the PHI(ACV) line.

4.12.1 100V Range Power Routing
(Circuit Diagrams: 430450 pages 7.9-2 and 7.9-3; 430447 page 7.7-1)

'AC1V' enters the Power Amplifier assembly at J9-36 (page 7.9-2). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL4 is energized, routing the AC1V signal to the 100V Amplifier as '100V I/P' (page 7.9-3).

Energized relay contacts RL2-8/4 apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via R89, L7 and relay RL2-13/9, to RL3-6 (page 7.9-2), and onto the 'AC 10V+100V' line via RL4-4/8.

On the AC assembly (page 7.7-1), the signal is routed to the PHI(ACV) line as for the 10V range.

4.12.2 100V Power Amplifier

The 100V amplifier is in three stages:

(1) **Gain Stage:** this is similar to the first stage of the 10V amplifier, but with a different distribution of gain.

(2) **Driver Stage:** providing most of the gain, this stage runs from a regulated 400V supply.

(3) **Buffer Output Stage:** two complementary MOSFET circuits, located on the positive and negative heatsinks, provide a single-ended output with the required voltage swing, at low impedance.

The voltage gain for the whole 100V amplifier is set at 100 by the input resistors R74/R71 and the feedback resistor R88.

The 100V amplifier is also used on the 1000V range to drive the step-up transformer.

4.12.3 Gain and Driver Stages
(Circuit Diagram 430450 pages 7.9-2 and 7.9-3)

The AC1V signal enters the PA assembly at J9-36, passing to the input of the 100V Power Amplifier via relays RL4-9/13 and RL2-8/4. It is referred to common 2B by developing a voltage across R72.

4.12.3.1 DC Offset Correction

Integrator M10 is the DC input amplifier, with diode clamping. It provides a DC input to the non-inverting input of the AC input amplifier, M8, controlling its DC offset. This is similar to the arrangement in the 10V Amplifier.

4.12.3.2 AC Signal Processing

M8 is a high speed hybrid amplifier operating as an inverter. With link LKD normally made, its stage gain is approximately 2.5, frequency compensated by C18 and C72. It operates from the ±15V Common-2B supplies, but its signal output is converted into a current by Q10 and Q8; allowing its mean DC voltage to reach the −400V levels required to operate the driver MOSFET output circuit. Diodes D44, D43 and D36 prevent negative latch-up.

Voltage Regulator M21 sets its pin 1 to +12V. Common-emitter buffer Q10 drives the capacitance of Q8 source-gate from the output of M8, forming a cascode current generator. The drain of p-channel MOSFET Q8 passes the signal current to the mirror Q12/Q11 at voltages close to −400V.

The current-mirror output transistor M11 is also in cascode with its associated MOSFET Q9. Emitter resistor R53 defines the current in Q9, the ratio R52/R53 setting the mirror's current gain.

MOSFETs are inherently capacitive, so measures are taken to nullify the effects, on slew rate, of the capacitive currents between Q9 electrodes. The cascode arrangement ensures that any source-gate and source-drain capacitive currents join the main flow of source current and have little effect on slew rate.

The Miller feedback of the drain-gate capacitance has the greatest effect on slew rate, generating AC currents between anti-phase electrodes which normally pass into the input circuit. In this arrangement, Q13 diverts these currents back into the cascode current, while maintaining a standing bias of about 4 volts between gate and source. Both these measures minimize the reduction of Q9 operating bandwidth.

R51 and D42 provide Q13 base bias, and D51 protects the bias curcuit. The high-power resistor R49 refers the bias circuit to Common-2, and C26 stabilizes the base-emitter bias of Q13. Zener diode D39 protects the MOSFET from source-gate voltage breakdown.

4.12.3.3 Driver Regulator

At Full Scale on the 100V range, the output from the driver is 200V RMS. This requires Q9 drain to provide a peak-to-peak voltage swing approaching 600 Volts, as there is no voltage gain in the heatsink power amplifiers. The positive supply which provides Q9 current therefore needs special regulation.

The 400 volt supply is at this point unregulated, so can contain line ripple and level variations, this noise level being critical to the output performance. To define a stable supply voltage, a DC restoration circuit is employed as a trough detector, maintaining a level about 5V below the most negative excursions of the ripple.

At power-up, 75V zener D57 allows a rapid charge of reservoir capacitors C49 and C59, until the charge reduces D57 voltage below the avalanche level. When D57 cuts-off, R100 provides a charge path of 1Mohm, giving a time constant of approx. 10 seconds. The smoothed voltage across C49/C59 is divided by R101, R86 and R87; so a small voltage is dropped across R101, and M20 gate is held about 5V below the +400V(2)B line voltage. The N-channel source-follower Q20 thus provides a quiet, low-impedance DC supply voltage.

Zener diodes D60 and D61 divide the voltage across C49 and C59, so that their breakdown voltages are not exceeded. The 10V zener D54 protects the TMOS gate/source from excessive voltages. D55 is included to prevent C49/C59 discharging into the 400V rail in the event of its being shorted.

The opto-coupler M16 permits the 400V supply to be switched off, allowing D56 to assume forward bias, connecting the rail to the +38V supply. This facility is not available on the 4200 AC calibrator, the 'POSITIVE' signal from the processor being permanently set to logic-1 (0V). Thus M16-6 is isolated from M16-5.

At HF, inductor L6 appears as a current source, increasing the impedance of Q9 drain load with frequency to compensate for capacitive loading. It has the advantage of not increasing the net power dissipated in the stage; any active current source would have significant output capacitance. The 12-watt resistor R65 is the main resistive drain load for Q9.

4.12.3.4 Driver Output

The driver develops its output voltage, which can involve peak-to-peak swings of up to 600V, across the load resistor R65. Zener diode D41 is included to clamp the output in the event of the heatsinks being disconnected. This is normally held below avalanche by the current passing through a series bias divider in the Positive Heatsink assembly, via J3-11 and J3-12.

The main frequency compensation is performed by capacitor C12. This could have been connected to the drain of Q9, but the output line slew rate is sensitive to capacitive loading. Instead it is connected via J2-7 to a low impedance point in the Negative Heatsink assembly, which follows the driver output voltage swing.

4.12.4 100V Buffer Output Stage

(Circuit Diagrams 430538 page 7.13-1 and 430539 page 7.13-2)

The 100V buffer output stage is split between the Positive and Negative Heatsink assemblies. The driver output voltage is connected into the Positive assembly, and the frequency compensation feedback is derived in the Negative assembly.

The whole circuit is a complementary, single-ended push-pull amplifier with unity voltage gain. To achieve the full ±300V peak voltage output, two MOSFET source-followers are connected in cascode, for each polarity, in a totempole arrangement.

To obtain the required peak current levels, each source-follower consists of two MOSFETs in parallel. In all, therefore, eight MOSFET devices are used.

On the 100V range, the output currents are such as to bias the amplifier in class A, but on the 1000V range the output currents impose class AB conditions. Crossover distortion is minimized by a regulated bias generated by a Vbe multiplier.

Power for the amplifier is provided by the same ±400V supply that serves the driver circuit. To improve efficiency, overall power loss is reduced by regulation only where required. Thus only the driver stage is regulated, allowing the power amplifier to take power directly from the unregulated supply. Being source-followers, the 400V rail ripple is not transmitted.

4.12.4.1 Positive Heatsink Assembly

(Circuit Diagram 430538 Page 7.13-1)

N-channel MOSFETs Q1 and Q2 are connected in parallel, as are Q3 and Q4. All devices are matched for power dissipation and threshold voltage for an even dissipation of approx. 400W between the two heatsinks. All gate-source potentials are limited by 10V zeners.

The input voltage swing from the driver is present at J3-11 and J3-12, and the driver load current passes through resistors R18, R17 and the bias control R10. The Vgs multiplier Q5 acts as a shunt regulator, generating a bias of between 5V and 9V, set by R10. Zener diode D7 responds to the temperature of the heatsink to compensate for the temperature coefficients of the MOSFETs.

The 'DRIVE−' voltage at J3-11 is transferred directly to the negative heatsink input via J1-7 (Circuit Diagram 430539 page 7.13-2).

The 'DRIVE+' voltage at J3-12 is buffered by Q7 and applied to the gates of Q3 and Q4. In the event of an output short-circuit, Q6 detects the output current as a voltage across R14, imposing a hard limit of 1.5A by reducing the signal voltage at the input to the MOSFET gates.

The series gate resistors R5 and R6, together with their associated drain-gate capacitances, form the dominant pole of the amplifier. Damping resistor R19, with ferrite bead FB1, prevent local oscillations by emitter-follower Q7.

Q1 and Q2 act as buffers to provide a bootstrapped supply for the output devices Q3 and Q4. The gates of Q1 and Q2 are driven from the output line, obtained from the divider R16/R22/R23/R15. Capacitors C10 and C13 decouple any noise on the 400V rail; C11 and C12 correct any lag which may be generated by C10 and C13. C5 and C6 control the division ratio at HF, swamping any stray capacitance.

The drains of Q3 and Q4 are shorted together, and connected via J1-5 by a 10nF capacitor to the corresponding point in the Negative Heatsink, completing an AC bootstrap (BS). J1-4 and J1-1 are similarly linked to their corresponding points. This ensures that the AC swings in both polarities are identical.

The combined output from the Positive and Negative Heatsinks is transmitted back to the Power Amplifier assembly along the screen of the input connection.

4.12.4.2 Negative Heatsink Assembly

(Circuit Diagram 430538 Page 7.13-2)

This is virtually a mirror image of the positive heatsink circuit. However, because the P-channel MOSFETs are operating closer to their maximum voltage rating, they are protected by Zener diodes which limit their gate-source potentials.

The HF swamp capacitors are not required, as the whole circuit is AC-bootstrapped to corresponding points in the positive heatsink assembly, via C1, C2 and C4.

HF compensation for the driver and output stages is derived at low impedance from the junction of R2 and D12. It feeds back via J2-7 to the driver output circuit, through C12 in the Power Amplifier assembly, to avoid capacitively loading the driver output line.

4.12.4.3 Over-Temperature Detection

The two NTC thermistors in each heatsink circuit are part of a bridge network which detects excessive temperatures on the heatsinks. The action of the bridge is described in section 4.12.9.6.

4.12.4.4 100V Output Connection

DANGER **For guarding purposes, the output from the heatsinks is transmitted back to J3-9 of the Power Amplifier assembly along the screen of the input cable.**

The voltages on this screen are POTENTIALLY LETHAL. Utmost caution should be exercised when working in its vicinity.

4.12.4.5 Heatsink Removal

The 100V Amplifier can work with the heatsinks removed, because of the clamp diode in series with the driver load. If they are removed, however, J3-9 must be connected to J3-11 to maintain the feedback. In this condition, the gain falls due to loading of the driver by the AC assembly.

4.12.5 1000V Range Power Routing

(Circuit Diagrams: 430450 pages 7.9-2 and 7.9-3; 430447 page 7.7-1; 430565 page 7.14-1)

'AC1V' enters the Power Amplifier assembly at J9-36 (page 7.9-2). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL1 is energized, routing the AC1V signal to the 1000V Amplifier chain.

Energized relay contacts RL1-8/4 apply the signal to the Gain X2 Stage, whose output is summed with error feedback, providing drive to the 1kV Error Amplifier.

The 1kV Error Amplifier output is passed as '1kV ERROR O/P' via relay RL1-9/13 to the 100V Amplifier (page 7.9-3). It is input through the contacts of un-energized relay RL2-6/4.

The heatsink output J3-9 is transferred directly, as the 'OUTPUT' signal, to the 1kV ENABLE relay contacts RL6-8 and RL6-9. Relay RL7 determines whether the LF or HF transformer assembly is to be used, the OUTPUT signal being applied to the appropriate primary winding.

The secondaries of both transformers are connected into the High Voltage assembly (page 7.14-1). Relay RL2 or RL3 selects the appropriate output to be passed on to the AC assembly, via J1-28 and J1-22, as the AC 1kV signal.

The AC 1kV signal is also applied as the negative 'Error' feedback to the 1000V amplifier system. It passes through R138 and R155 on the PA assembly (pages 7.9-1 and 7.9-2), to be summed at the inverting input of M18a-2. A single net inversion is present around this loop.

On the AC assembly (page 7.7-1), the AC 1kV signal is routed by the contacts of energized relay RL20, and through fuse F2 to the PHI(ACV) line at J7-27.

4.12.6 1kV Power Amplifier

(Circuit Diagram 430450 page 7.9-1)

Amplification to a maximum of 1100V is in four stages:

(1) **Gain X2 Stage:** the AC1V signal is HF-boosted and amplified. For the 1000V range the DC Reference is scaled in software, so that the AC1V signal Full Scale value represents 1100V output.

(2) **1kV Error Amplifier:** the Gain X2 Stage output is summed with error feedback from the secondary of the step-up transformer.

(3) **100V Amplifier:** possessing a gain of 100, the output from its heatsinks drives one of two (LF or HF) step-up transformers.

(4) **Step-up Transformer:** a ratio of 1:6 allows sufficient gain in the system to provide a maximum RMS output of 1100V.

The frequency response of the amplifier is matched to the step-up transformer in use. The 'LF' signal into the amplifier is at logic-1 (0V) only when the 1kV range, and either the 100Hz or the 1kHz frequency range, is selected.

4.12.6.1 Gain X2 Stage

(Circuit Diagram 430450 page 7.9-2)

The AC1V signal is routed via relay RL1-8/4 to be developed across resistor R160. It is filtered by R162/C30 and applied to the non-inverting input of M15.

The feedback divider generates the X2 gain in M15; R159 and C67 providing HF lift. FET Q35 adds C68 on the 100Hz and 1kHz frequency ranges, activated by the LF signal at logic-1, to boost the lift.

Output from the X2 stage is applied to the 1kV Error Amplifier via its input resistors R156/R95.

4.12.6.2 1kV Error Amplifier

The input resistance to M18a is split between R156 and R95 to allow the saturation detector to reduce the gain in the event of transformer saturation.

At the inverting input of M18a the signal input is summed with the AC 1kV negative feedback signal, output from the selected transformer secondary. The resulting error is amplified by the 2 stages of M18.

On the 100kHz frequency range, the maximum voltage available from the instrument is 750V. A tapping on the HF step-up transformer secondary reduces the maximum output to this level. The signal '1kV GAIN' is therefore set to logic-Ø only on the 100kHz range, cutting off FET Q19 and restoring adequate loop gain.

The second stage, M18b, adjusts the bandpass of the amplifier to match the selected step-up transformer:

100Hz and 1kHz ranges:
Q26 connects C58 and R126 across the input resistor R97; relay RL5 connects C34 and R93 across the feedback resistor R92, also shorting C38 in the output line.

10kHz and 100kHz ranges:
Q26 connects C57 and R125 across the input resistor R97; relay RL5 connects C33 and R94 across the feedback resistor R92, and leaves C38 dominant in the output line.

These measures give the necessary loop compensation for each transformer.

When the 1000V range is selected the amplifier output is fed to the 100V Amplifier via RL1-9/13.

4.12.6.3 100V Amplifier

This operates as for the 100V range, and its output signal 'OUTPUT' is fed to relay RL6 contacts for application to the step-up transformer.

4.12.6.4 '1kV ENABLE' Relay RL6

Relay RL6 allows the OUTPUT signal from the 100V Amplifier to energize a step-up transformer, providing the following conditions are met:

The $\overline{1kV}$ signal is at logic-Ø:
This is a processor-controlled signal, set to logic-Ø when the 4200 output is switched on, in the 1000V range.

The watchdog has not 'Barked'.

The '1kV ENABLE' switch S1 on the Power Amplifier assembly is set to 'ENABLE'. S1 is situated below the left-hand ejector lever (viewed from the front of the 4200), facing the rear of the instrument. It allows the high voltage to be switched off for servicing purposes. A red LED glows when all other conditions are met.

When RL6 is closed, the OUTPUT signal from the 100V Amplifier is switched through to the contact of RL7.

4.12.6.5 LF/HF Transformer Selection

Relay RL7 is activated by the 'LF' signal, applying the 100V amplifier output to the HF step-up transformer for the 10kHz and 100kHz frequency ranges, and to the LF transformer for the 100Hz and 1kHz ranges.

The two transformer are separately located, their secondaries being connected into the High Voltage assembly. The HF transformer is selected when RL7 is un-energized, its primary being returned to Common-2C. RL7 is energized to select the LF transformer, whose primary current is sensed by the Saturation Detector.

4.12.6.6 Saturation Detector

To obtain the required performance, the LF transformer core is constructed from a material with high remanence. It is possible for the 1kV range to be deselected when the core is magnetized, and subsequently reselected in the same sense, with resultant saturation.

The Saturation Detector circuit is activated by sensing any excess primary current in R114, associated with the loss of reactance. It progressively removes the signal input to M18b during half cycles of the appropriate sense until the core recovers, then automatically returns to its quiescent mode.

The dual amplifier M20 is biassed by R115-R118 to approximately 1V on each input. Under normal operating conditions, the unsaturated core reactance holds R114 current down, so the voltage developed across R114 is insufficient to overcome the bias. The output from both amplifiers is of negative polarity, both diodes D58 and D59 are reverse-biassed, and FET Q18 is cut off by its gate being pulled down to −15V.

When the core saturates, the current in R114 rises rapidly and its voltage exceeds the bias on one of the detector amplifiers. One diode conducts, forcing Q18 into conduction, so the current in the transformer core is reduced to zero.

On the next half-cycle the current is reversed, so saturation is reduced. If the core saturates on successive half-cycles, they again activate the detector with further reduction. The process continues until the core remains unsaturated over the full dynamic range of the primary current, when the detector becomes inactive.

4.12.7 Power Supplies and Protection

Three main power supplies are employed in the Power Amplifier:

(1) **± 15V Common-2 in-guard supply.**
This is used for all low voltage applications, including the switching and functional logic. For the most part the logic conforms to the standard: logic-0 = −15V; logic-1 = 0V.

(2) **± 38V Common-2 supply.**
Required solely for the 10V Power Amplifier, this supply is generated on the separate 38V Power Supply assembly (Refer to page 7.12-1). Part of the supply circuit is situated on the Mother Assembly.

(3) **± 400V Power supply.**
Supplies the 100V Power Amplifier used for the 100V and 1000V ranges. The line transformer secondary output is rectified and smoothed on the Mother assembly, and the main regulator circuitry for the driver stage is contained on the Power Supply / Current Heatsink. The power output stage of the 100V Amplifier receives unregulated ± 400V supply.
Extensive protection is incorporated.

4.12.7.1 ± 38V Supply
(Circuit Diagram 430544 Page 7.12-1)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly after passing through the 38V Power Supply assembly. This secondary also provides an adjustable AC output for the 'Common Mode Null' balancing circuit.

A single bridge rectifier on the Mother assembly provides both positive and negative raw supplies for the foldback regulator in the 38V Power Supply assembly.

The 38V supply circuit is fully described in Section 4.16, para 4.16.3.4.

4.12.7.2 ± 400V Transformation and Rectification
(Circuit Diagram 430532 Page 7.16-5)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly. The secondary is switched with the secondary for the ± 38V supply, to allow a lower voltage to drive the 100V power amplifier for servicing purposes. Under operational conditions in the 4200, this switch, which is situated prominently on the Mains Transformer assembly, is set to the 400V position.

A single bridge rectifier on the Mother assembly uses series diodes to achieve the high peak inverse voltage performance required for the 400V supply.

After smoothing, and part-loading by a bleeder resistor chain (the bleeder resistors also balance the voltages across the capacitors); the rectifier output is passed via J31, to provide both positive and negative raw supplies for the foldback regulator in the PS/I Heatsink assembly.

4.12.7.3 ± 400V Current Control
(Circuit Diagram 430540 Page 7.13-3)

When the 400V supply is enabled, the LEDs in opto-isolators M1 and M2 are conducting, allowing their opto-transistors to be energized. As the circuits for both polarities are otherwise symmetrical, only the positive circuit is described.

Zener Diode D8 protects the source-gate circuit of level-shifter Q3. This N-channel MOSFET supplies a current of 1.4mA, as defined by Q8, to the current-monitor reference zener diode D7. This current is available only if the 400V supply is enabled by M1, otherwise Q4 base is pulled down by D1/R9, Q4 conducts via D7 and Q9 is pinched off.

Under normal conditions the Power Amplifier supply current is drawn through the P-channel MOSFET Q9, which is held in conduction by R8, R12 and D2. The current is sensed by the parallel combination of resistors R17 and R32. Although the peaks of the current taken by the power amplifier can reach 1.4A, the mean value is less than 0.5A. Ripple currents making up the difference are smoothed by the main reservoir capacitors C31 and C22 on the Power Amplifier assembly.

For mean currents more than approximately 0.5A (in particular for output short-circuits); the voltage sensed across R17/R32, subsequently divided by the attenuator R10/R9, exceeds the threshold of Q4/D7. Q4 conducts to pass current into R8, reducing the drive to Q9 gate, so the +400V(2)B voltage at D5 anode falls. When the voltage dropped by Q9 reaches 56V, zener D5 conducts and pulls Q4 base down, further reducing the drive to Q9 gate. This cumulative action is slowed only by the time constant of the combination R34/C15, so that both voltage and current on the +400V(2)B line are simultaneously closed down.

With a persistent 400V overload, the circuit cannot recover naturally from this 'foldback' mode. However, the 400V voltage is monitored. If the 400V monitor senses a failure, a status bit is passed back to the CPU via the SSDA serial link. The CPU makes three attempts to reinstate correct operation by removing the PA bias while restarting the supply via the 400V enable line. If after the third attempt the voltage does not recover, the CPU assumes that a hardware fault is present, so displays the 'FAIL 7' message.

4.12.7.4 100V Overload Detector

(Circuit Diagram 430450 Page 7.9-6)

The ±400V(2)B lines enter the Power Amplifier assembly from the PS/I Heatsink at J1-8/6 and are filtered by L1 and L2 before being applied across two neon lamps LP1 and LP3. These lamps are visible from the top and rear of the instrument when the PA board is exposed, indicating that a dangerous voltage is present.

The 400V(2)B lines continue on to power the driver stage of the 100V amplifier, where the voltage is regulated as described in sect 4.12.3.3.

The ±400V(2)C lines supply the power amplifier in the Positive and Negative Heatsinks. On the 100V range, the current in each of these lines is used as an analog of the load placed on the amplifier. (On the 1000V range, any overload is sensed by a series detector in the OUTPUT control assembly.)

The '100V A' line is set to logic-1 (0V) only when the 100V range is selected ('100V D' is not used in the 4200). Driver Q7 pinches off the two FET switches Q6 and Q37, removing the shorts from R37 and R21, thus allowing the overload detector to operate. In normal use, links LK B and LK C are not connected. Their test purpose is to allow the current mirrors Q1 and Q3 to be powered without the level-shifters Q2 and Q4.

Most of the positive output current for the heatsinks passes through the series combination of R34 and D27, the negative currents through R9 and D4. As the both positive and negative circuits are symmetrical, only the positive circuit is described.

Current mirror Q3 diverts approx. 1.8% of the positive supply current into the level-shifter Q4, R36 and into the common resistor R37. Similarly Q1 draws current out of R37. Under no terminal load conditions these two currents are balanced, even if the output voltage is high.

Any AC output load current from the power amplifier is reflected by ripple currents in both positive and negative supplies. The net instantaneous current flowing in R37 alternates in synchronism with the output cycles, its amplitude increasing as the load current increases. So the amplitude of the alternating voltage across R37 is an analog of the output load current, and can be compared against a scaled reference voltage.

A window comparator is formed from the two halves of M2 and the voltage across R37 is applied to both halves. The outputs at M2-12 and M2-7 are uncommitted. Each half is biassed by approx. 1.025V in the correct polarity, so that unless any voltage peak across R37 exceeds this level, both M2 outputs will be pulled to 0V by R21. So Q9 remains cut-off.

Any peak greater than 1.025V ovrcomes the bias on one half, causing its output to fall to −15V, so Q5 conducts, lifting TP2 to 0V (logic-1). Diode D13 is part of a wired-OR gate which then sets the limit detector latch M5a (page 7.12-5), resulting in the $\overline{\text{LIM ST}}$ status bit being set to logic-1. This is passed to the CPU via the SSDA serial link. Meanwhile the LIM DET signal passes via D38, becoming the 'I LIM 100V AMP' signal to Q14 (page 7.12-3) in the gain stage of the 100V amplifier. Q14 conducts, shorting the input to the amplifier to Common-2, and reducing the amplifier output.

The CPU tries to toggle the latch, and will succeed once the overload is removed. While it is clocking the toggle with 'I LIM RST', it displays the message 'Error OL'. Note that the action described trips the output off. Thus removing a terminal overload will not restore the output.

4.12.7.5 1000V Overload Detector

(Circuit Diagram 430550 Page 7.5-1)

For the 1000V range, so as to protect the step-up transformers, overloads are detected directly in the output lines to the terminals. For this range only, two resistors are inserted in the PHI(V) line in the Output Control assembly. The voltage across the resistor is rectified and compared against a reference. If the voltage is excessive, the comparator generates a LIM DET signal.

The 'AC 1kV RANGE' signal enters at J5-102. This is at logic-1 to energize relay RL1, only if the 1000V range is selected. RL1 removes the short from R31 and R32.

The 'HIGH I LIMIT' signal enters at J5-98. When the 1000V range is selected, this is at logic-1 only for the 10kHz, 100kHz and 1MHz frequency ranges. It energizes relay RL2, shorting R32, so that higher currents are required to trip the LIM DET signal. As frequency increases, so do the currents taken by the capacitance of the internal tracking and wiring; R31 is compensated by C16 to bypass this capacitive loading.

A diode-bridge rectifies the voltage developed across the selected resistor(s). The voltage is limited to 10V by D14, and resistor R33 sets the trip current level for the opto-isolator M8.

The isolator operates from the 5 volts between −10V and −15V. In normal operation M8 output at M8-6 is open-collector so Q5 does not conduct. When the output current is sufficient to trip M8, Q5 emitter is pulled low and so Q5 conducts, its collector current being drawn through R21 and R20 (page 7.5-2). Q4 is switched on, setting the LIM DET line to logic-1.

4.12.8 PA Power Supply Monitors
(Circuit Diagram 430450 Page 7.9-4)

All three power supply voltages: 15V, 38V and 400V; are monitored using three virtually identical comparators to initiate individual 'FAIL' messages. In addition, if either the 400V or the 15V circuit detects a low power supply voltage, the 400V supply is disabled. Because the monitors are so similar, only the 400V circuit is fully described.

4.12.8.1 400V Monitor

Zener diode D5 is the 2.45V reference for all three comparators. It is ballasted by R30, and its +2.45V is applied to the non-inverting input of M3d. Its voltage is divided equally by two sections of AN3, applying +1.23V to the inverting input of M3a.

The +400V(2)B line voltage is divided down to approximately 3.25V by R3 and R16, and applied to the inverting input of M3d. This is sufficient to hold M3d-14 output negative. Diode D20 is held below threshold by R7 and a 1Mohm pull-up on the 400V(2) status line in the Reference Divider. If the +400V line voltage falls to 300V, M3d output goes positive, limited by D6. D20 conducts, setting the status line to logic-1 (0V), positively limited by D8.

The −400V(2)B line voltage is similarly divided down to approximately +0.9V by R4 and R26, and applied to the non-inverting input of M3a. This is sufficient to hold M3a-1 output negative. Diode D23 is also held below threshold. If the −400V line voltage falls to −315V, M3a output goes positive, limited by D7. D23 conducts, again setting the status line to logic-1 (0V).

The output line gives an input to the 400V enable logic (sect 4.12.9.4).

In normal 400V operation R31 is shorted by the 400V/50V switch on the Mains (line) transformer. When this is set to 50V, the 'Lo SUPPLY A' line is connected to −15V, effectively disabling the monitor output by holding the 400V(2) line at logic-Ø.

4.12.8.2 38V Monitor

The thresholds for operation of the 38V fail flag are: +32V and −33V. Otherwise the action is the same as the 400V monitor.

4.12.8.3 15V Monitor

The thresholds for operation of the 15V fail flag are: +12.05V and −12.3V. The action is similar to the 400V monitor, but because the 15V circuit is running from the supply it is monitoring, extra precautions are required and the action is slightly modified.

Under normal operating conditions, D21 and D22 are reverse-biased, so the 15V(2) FAIL line is pulled to logic-Ø by R17.

If the −15V supply fails, the action is as before, but in this case it is assisted by M3 power supply being between +15V and 0V. D22 will conduct to drive the 15V(2) FAIL line to logic-1.

On the other hand, if the +15V supply fails, the reference supply to D5 would collapse and both amplifiers would run between 0V and −15V (D32, shown on page 7.9-6, prevents the +15V line reversing). The 2V zener D16 then ensures that as the +15V supply collapses, M3c-9 is pulled more negative than M3c-10 at all times, regardless of supply levels. Thus M3c-8 output is driven to its positive rail, which can source enough current to hold the 15V(2) FAIL line at logic-1.

The 15V monitor output line also gives an input to the 400V enable logic (sect 4.12.9.4).

4.12.9 PA Logic and Relay Drives
(Circuit Diagrams 430450 Pages 7.9-4 and 7.9-5)

The CMOS logic operates between 0V and −15V, with logic-1=0V, and logic-Ø=−15V. Relays are tied to +15V on one side, and controlled on the other by the uncommitted collector of an inverting Darlington driver. Thus when the input to the driver is logic-1, the relay is energized by ± 15V; and when the driver input is logic-Ø, its output is high impedance, releasing the relay.

4.12.9.1 Range Switching
(Page 7.9-5)

In the 4200, the inputs to decoder M7a are not connected outside the PA assembly. They are therefore all pulled to logic-1 by AN4, including the 'E' input, so all 'Q' outputs are at logic-Ø.

The three inputs AC RØ, AC R1, AC R2; carry the range switching information, and are decoded by M7b as follows:

	M7b outputs			M7b inputs		
	Q2	Q1	QØ	E	B	A
Range Select	AC R2	AC R1	AC RØ			
1000V	Ø	Ø	Ø	Ø	Ø	1
100V	Ø	Ø	1	Ø	1	Ø
10V	Ø	1	Ø	1	Ø	Ø
1V	Ø	1	1	Ø	Ø	Ø
100mV	1	Ø	Ø	Ø	Ø	Ø
10mV	1	Ø	1	Ø	Ø	Ø
1mV	1	1	Ø	Ø	Ø	Ø

10V Range Logic

The input to Q6-1 is always logic-1. On the 10V range only, the input to Q6-2 is logic-Ø, giving logic-1 at M6-3. Thus relay RL3 operates only when the 10V range is selected.

100V Range Logic

The input to Q12-8 is logic-Ø only when the 10V range is not selected, and the input to Q12-9 is logic-Ø only on the 100V range. This gives logic-1 at M12-10, so relay RL2 operates only when the 100V range is selected.

1000V Range Logic

The input to Q13-4 is logic-Ø only when the 1000V range is selected, so relay RL1 operates only when the 1000V range is selected. An 'AC 1kV RANGE' signal is also passed to the Output Control assembly to select the overload sense resistor.

4.12.9.2 Range-Changing Logic

In the 4200, the input to M12-13 is held permanently at logic-Ø. Except during range changes, the $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ signals are always of opposite logic. Although M7a-4 is always at logic-Ø, the logic-1 from M6-11 is sufficient to energize relay RL4. During range changes both function signals are driven to logic-1, momentarily releasing RL4.

4.12.9.3 1kV Enable Logic

With the 1000V range selected, and if the watchdog has not 'barked', M12-3 is at logic-1 and LED D70 is lit. Relay RL6 is energized if the 1kV ENABLE switch on the PA assembly is set to ENABLE.

For other ranges, or if the watchdog barks, RL6 is de-energized, removing the AC drive to the step-up transformers. LED D70 is also de-energized.

4.12.9.4 '400V ENABLE' Logic

The '400V(2) OFF' signal from the CPU is normally at logic-Ø for voltage ranges; but after a 'FAIL 7' message indicates a 400V supply failure, it is toggled three times, attempting to restore the supply.

In normal operation, therefore, with BARK at logic-Ø, the PS1 OFF signal from M11-4 is also at logic-Ø, and is input to M1-1/6 (page 7.9-4). M1 consists of six inverting drivers, each with uncommitted-collector output (as used for the relay drivers). M1-1 at logic-Ø allows M1-2 to be pulled to logic-1 by AN1-1/2, or to logic-Ø by M1-14. In the lower chain with four inversions, M1-14 is also open-collector, if a 400V or 15V failure has not been detected by the monitors.

Thus for normal operation M1-2 is pulled to logic-1 and the 'ENABLE 400V–' line from M1-15 is held at logic-Ø (–15V). With the 'ENABLE 400V+' line it energizes the opto-isolator LEDs in the 400V power supply (PS/I heatsink page 7.13-3).

A failure of either the 400V or 15V supply pulls M1-3 to logic-1, disabling the 400V supply by setting the ENABLE 400V– line to logic-1. If the +15V or –15V rail collapses, the opto-isolator current is cut off in any case, due to zener D24.

4.12.9.5 'BIAS OFF' Logic

On the 100V or 1000V ranges, after receiving a 400V FAIL signal from the monitor, the CPU attempts three times to restore the 400V supply. The foldback current limiting for the supply (in the PS/I heatsink) prevents reinstatement if an overload persists. Thus it is necessary to remove the overload if the supply is to be restored. This is done by setting the BIAS OFF line to logic-Ø (–15V), cutting off Q10 (page 7.9-3) and removing the output drive.

The attempts are made by toggling the 400V (2) OFF line (described in sect 4.12.9.4). Each time the supply is enabled, R6 and C1 hold the BIAS OFF signal at logic-Ø for about 1ms to allow the supply to build up before the load is reapplied.

After three unsuccessful attempts, the CPU assumes a permanent hardware fault and holds the 400V (2) OFF signal at logic-1.

4.12.9.6 '$\overline{\text{LIM ST}}$' Logic

This status signal is passed back to the CPU via the SSDA serial link to indicate that certain limits have been exceeded. The $\overline{\text{LIM ST}}$ signal entering the Reference Divider assembly at J4-76 (page 7.4-6) can be activated to logic-Ø by any one of six detectors, as illustrated in the simplified diagram of Fig. 4.12.1.

The signal output from the Power Amplifier at J9-67 (page 7.9-2) can result from the LIM DET signal setting the latch M5a (page 7.9-5).

LIM DET is set to logic-1 by the 100V Overload Detector (page 7.9-6), if the 400V supply current peaks are excessive. It can also be set by the 1000V Overload Detector or Overvoltage Detector in the Output Control assembly (page 7.5-1/2). The logic-1 is immediately transferred via D38 as 'I LIM 100V AMP' to the gate of Q14 (page 7.9-3). Q14 conduction reduces the 100V amplifier input to zero, so if the overload is external the LIM DET signal should rever to logic-Ø.

The latch M5a is set by logic-1 on pin 6, for as long as LIM DET remains at logic-1. Its 'Q' output reinforces and latches the 'I LIM 100V AMP' signal. Its 'Q' output is the '$\overline{\text{LIM ST}}$' signal, so the CPU is informed. The CPU initiates a series of clock pulses on the 'I LIM RST' line via the SSDA and Reference Divider, so that M5a can be reset as soon as the LIM DET signal clears to logic-Ø, M5a 'D' input being strapped to −15V. The CPU also displays the 'Error OL' message.

If the LIM DET line has cleared to logic-Ø, the 100V Amplifier input is reinstated by M5a being reset. Furthermore, if the overload was temporary, the LIM DET line remains at logic-Ø, and operation returns to normal. The CPU is informed by $\overline{\text{LIM ST}}$ at logic-1, so the reset pulses are discontinued, and the Error message is removed.

For a persistent overload, the detectors operate once again. The cycle repeats until other user action is taken to remove the overload. The Error message continues to be displayed.

If the overload is an internal fault, it is likely that another protection circuit will have detected it and taken its own action.

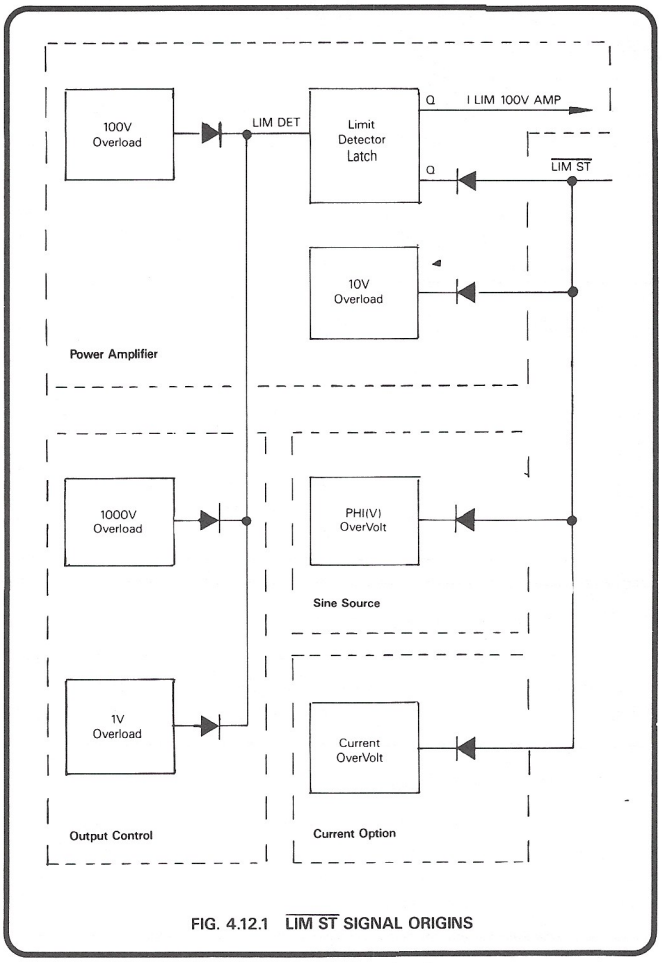


FIG. 4.12.1 $\overline{\text{LIM ST}}$ SIGNAL ORIGINS

4.12.9.7 'LF', '$\overline{\text{LF}}$' and '1kV GAIN'

These are signals used to control the gain and compensation of the 1kV amplifiers (Refer to section 4.12.6).

The 'LF' signal is set to logic-1 by the CPU via the SSDA serial link and Reference Divider latches, when the 1000V range and the 100Hz or 1kHz frequency ranges are selected. It is inverted as 'LF' at M11-12, and subsequently inverted as buffered '$\overline{\text{LF}}$' at M11-10.

'FREQ RØ' is also CPU-controlled. It is set to logic-1 when either the 1kHz or 100kHz frequency range is selected.

'LF' and 'FREQ RØ' are combined at M6-10 to give the '1kV GAIN' signal, which is at logic-Ø only when the 100kHz range is selected. (The software prevents the 1MHz range being selected on the 1000V range).

4.12.9.8 Thermistor Comparator

Two NTC thermistors situated in different positions on each PA heatsink are part of a bridge network which detects excessive temperatures on the heatsinks.
(Section 4.12.4.3 and pages 7.13-1/2 refer.)

The reference arm of the bridge is formed by R169 and AN9-7/10 in parallel, both in series with AN9-6/11.

The sense arm has four parallel sections, each consisting of one section of AN9 in series with one of the NTC thermistors. Four null detectors are used (M22 and M23), each comparing the voltage at the reference arm junction with that at the junction of one of the sections:

TEMP +R
TEMP −R
TEMP +F
TEMP −F

At 25°C each thermistor resistance is 10kohms. The bridge is unbalanced in favour of open-collector outputs from the four comparators, pulled up to Common-2 by R163 and R164. Q36 is therefore cut off, and the 'OVERTEMP' signal at J9-31 is at logic-Ø (−15V).

If one of the chip temperatures exceeds 100°C, its thermistor resistance falls to the extent that the bias on its null detector is reversed. The null detector output is taken low to −15V, Q36 conducts and the OVERTEMP signal goes to logic-1.

The OVERTEMP status signal is passed to one of the Reference Divider status registers, (page 7.4-4), where for safety reasons it is pulled-up by a 1Mohm section of AN2. The CPU reacts to the signal by displaying the 'FAIL 1' message, and forcing a recovery sequence:

OUTPUT OFF;
Reference Divider ramp to zero;
Remote Sense OFF;
Analog Control 'OFF' bit set;
Analog Control '1kV' line disabled;
Display and Keyboard locked;

After approximately 1 minute, the CPU defaults the instrument to the normal 'OUTPUT OFF' state in the selected ranges with output set to zero. The FAIL 1 message is removed, and the user is at liberty to make another attempt.

Under normal power-up conditions, with the Power Amplifier assembly plugged in and Q36 cut off, R167 holds the line more negative than −14V (logic-Ø). If the Power Amplifier is removed, no over-temperature information is available from the heatsinks. In this event, the OVERTEMP signal rises to logic-1, indicating failure.

4.13 HIGH VOLTAGE SENSING

(Circuit Diagram 430447 pages 7.7-1 and 7.7-2)

The SHI (ACV) signal, returned from the terminals via the Current and Output Control assemblies, enters the AC assembly as for the 10V range; but the 1V/10V Sense Amplifier is bypassed for the high voltage ranges.

On these ranges, the signal is switched into one of two guarded attenuators, both housed in the Attenuator/Cage assembly plugged directly into the AC assembly. Each attentuator is a separate resistor chain which acts as the input resistor to the inverting amplifier M32. The output of the amplifier is passed to the Comparator transfer switch.

4.13.1 100V Sense Amplifier

The SHI (ACV) signal passes through the contacts of energized relays RL19 and RL15, and is applied via the four pins of J1 into the 100V attenuator chain. The attenuator consists of four 25kohm 0.1% resistors in series. To guard out stray capacitance, each junction between the resistors is taken to an equivalent voltage point on a chain of four capacitors, C64 to C67. The capacitive chain is also driven from the sense signal.

Relay RL13 is un-energized on this range, so R124 acts alone as the feedback resistor, producing an amplifier gain of 1/100. The sense signals are thus reduced to 1V range levels. The amplifier output is routed through the contacts of unenergized relay RL3 as the comparator 'SIG' input, to transfer switch M16-11 (page 7.7-3).

4.13.2 1000V Sense Amplifier

The SHI (ACV) signal is blocked by the contacts of un-energized relay RL15, but RL16 is energized, applying the '1kV SENSE' signal via link LK1 into the 1000V attenuator chain. The chain has ten 50kohm 1% resistors in series. The guards are taken to equivalent voltage points on a chain of eight capacitors, C70 to C77, again driven from the sense signal.

Relay RL13 is energized on the 1000V range, so R123 and R124 act in parallel as the feedback resistance, giving a gain of 1/550. The sense signals are thus reduced to 1V range levels (the 1000V range FS voltage is 1100V; the equivalent 1V range voltage is 2V). The amplifier output is routed to transfer switch as for the 100V range.

4.14 Sine/Quasi-sine RMS Comparator

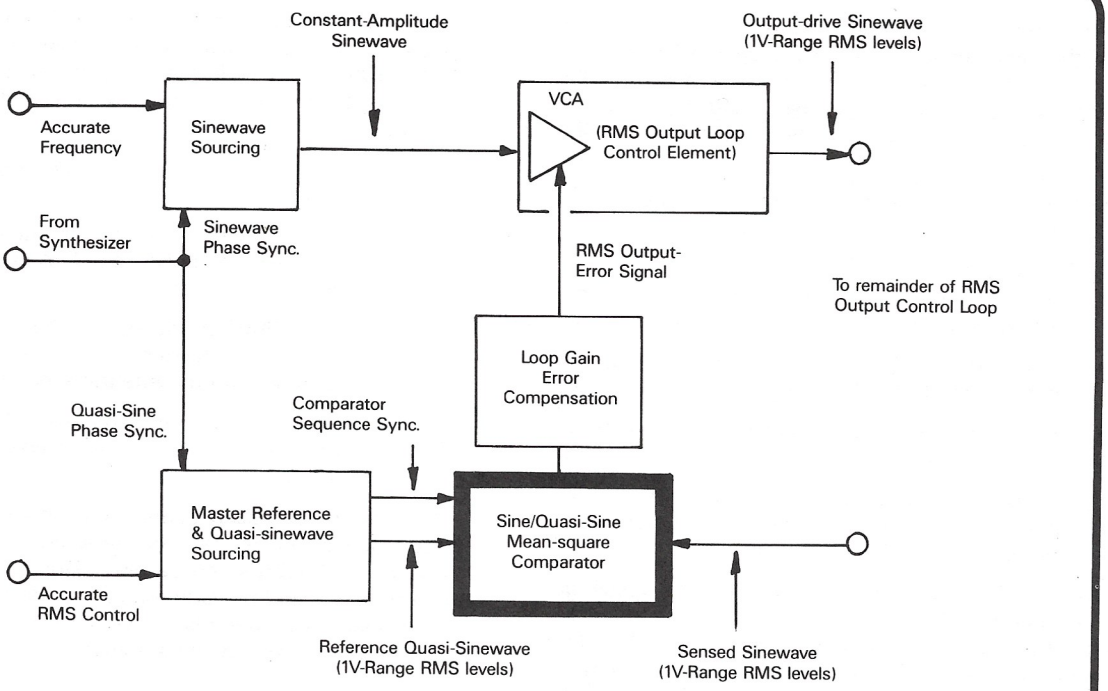


FIG. 4.14.1 THE SINE/QUASI-SINE COMPARATOR AND ITS SYSTEM ENVIRONMENT

4.14.1 Purpose and Environment
(Fig. 4.14.1)

The VCA acts as the control element of the Fine Amplitude Control Loop, having variable gain which is adjusted to change the 4200 output value.

The main purpose of the comparator, in conjunction with the coarse amplitude control, is to cause the 4200 output RMS value to track the value set on the front panel OUTPUT display. It generates a DC error voltage which adjusts the VCA gain.

Because it is part of the fine amplitude control loop, the comparator also corrects output RMS changes due to loading and other disturbances, within the instrument specification.

The Comparator receives two analog inputs:

a. The reference quasi-sinewave whose RMS value is set by the value on the OUTPUT Display, and is also modified by stored calibration data (Refer to section 4.6), and

b. The sensed and conditioned output sinewave (Refer to section 4.12), which is compared against the reference quasi-sinewave.

The Comparator output is the DC error voltage resulting from the difference between the RMS values of the two inputs. As the VCA gain (and hence the output RMS level) is adjusted, the RMS value of the comparator's sense input approaches that of the reference, and the error voltage is driven towards zero. The output value stabilizes when the RMS values of the two inputs are equal.

The buffered DC error signal output from the comparator is adjusted in approx. 1000ppm FS steps by the action of the Coarse Amplitude DAC, to give a virtually constant loop gain. The effects are described in sub-section 4.10.

4.14.2 Implementation

Both inputs are scaled to 1V Range levels and compared in an Integration/Sample-and-Hold system. They are sequentially steered through a common squaring circuit into separate 'REF' (reference^2) and 'SIG' (reference^2 minus sense^2) averaging integrators.

A capacitor and voltage follower samples and holds the settled REF integrator voltage. It generates a DC 'REF^2' signal which is subtracted from the AC 'SIG^2' signal. The result is applied to the SIG integrator, then another sample-and-hold circuit generates the 'AC ERROR' signal from the integrator's output.

'AC ERROR' is thus a DC analog of the difference between the 'mean-square' values of the two inputs. It is buffered and applied to the VCA via the Error Amplifier.

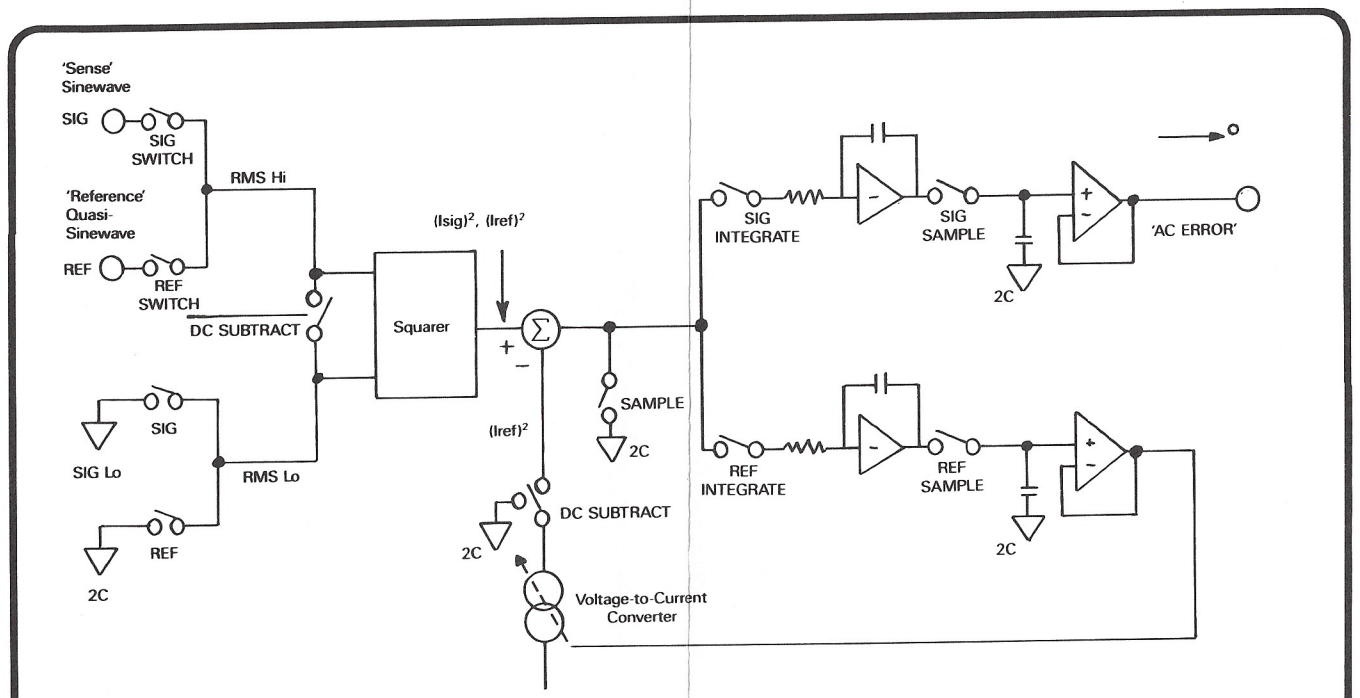


FIG. 4.14.2 SINE/QUASI-SINE COMPARATOR—BLOCK DIAGRAM

'X' indicates that switch is closed.	COMPARATOR CYCLING PERIODS									
	C 1	C 2	C 3	C 4	C 5	C 6	C 7	C 8	C 9	C Ø
States	REFERENCE PATTERN					SENSE (SIG) PATTERN				
(a) Squarer input	← quasi-sine →			zero		← sine →			zero	
(b) REF SWITCH	X	X	X							
(c) REF INTEGRATE	X	X	X	X						
(d) REF SAMPLE					X					
(e) SIG SWITCH						X	X	X		
(f) SIG INTEGRATE						X	X	X	X	
(g) SIG SAMPLE										X
(h) DC SUBTRACT	X	X	X			X	X	X		
(j) $\overline{\text{DC SUBTRACT}}$				X	X				X	X
(k) SAMPLE					X					X
(l) RMS Lo	COMMON-2C					SIG LO				2C

FIG. 4.14.3 SINE/QUASI-SINE COMPARATOR—SEQUENCE CYCLE

4.14.3 Method of Comparison
(Figs. 4.14.2 and 4.14.3)

The comparator is based on a ten-state recycling sequence of squaring, integration, sampling and subtraction. Operation and accuracy rely heavily on synchronization between sinewave and quasi-sinewave.

At relevant points in the following description, reference is made to a specific output frequency of 500Hz (1kHz Range), as an example to clarify the following points:

a. As the output sinewave frequency is varied, the quasi-sinewave tracks an exact sub-multiple of its frequency; except on the 100Hz Range, where both are at the same frequency. In our example at 500Hz, the quasi-sinewave has half the output frequency.

   The various relationships between output and quasi-sinewave frequencies for different frequency ranges are detailed in Section 4.7, Table 4.7.3.

b. The duration of each comparison cycle is always equal to ten quasi-sinewave periods (here 40ms), and each of the 'C' periods persists for one quasi-sinewave period (for 500Hz output—4ms). This effect can be observed using an oscilloscope, say at TP46.

c. Using this specific case also gives a point of reference for examination of the circuit waveforms using an oscilloscope.

4.14.3.1 The Comparator Sequence
(Figs. 4.14.2 and 4.14.3)

The table in Fig. 4.14.3 shows the conduction patterns of the switches in the block diagram of Fig. 4.14.2, within a complete sequence cycle. The cycle is broadly divided into two similar patterns ('REF' and 'SIG'), each occupying five quasi-sinewave periods. The cycle repeats continuously.

In the following analysis, the effects of the closed switches are described; all other switches are open.

Periods C1, C2 and C3

a. REF SWITCH is closed to input the quasi-sinewave to the squarer.

b. REF INTEGRATE steers the squarer output current into the Reference Integrator.

c. DC SUBTRACT allows Isub to be drawn from the summing junction.

d. RMS Lo has been connected to common 2C since the start of CØ in the previous period, in preparation for REF squaring.

The quasi-sinewave is squared, and the result is output as a current (at twice the input frequency) into the summing junction. The DC current Isub is subtracted at the junction, and the residue goes to charge the Reference Integrator capacitor.

(Note that every time the 4200 OUTPUT OFF is selected, REF and SIG integrator capacitors are discharged, driving both 'AC ERROR' and 'Isub' to zero. During the first REF integration when OUTPUT ON is next selected, Isub remains at zero so the integrator capacitors start charging from zero.)

Period C4

a. REF SWITCH is opened, removing the input to the squarer.

b. DC SUBTRACT is opened, subtraction ceases.

c. $\overline{\text{DC SUBTRACT}}$ closes to input a hard zero to the squarer.

d. REF INTEGRATE remains closed, allowing the squarer and integrator to settle.

e. RMS Lo remains connected to common 2C until the integrator has settled.

The REF integrator remains in its integrating (on) condition during period C4, to ensure that any energy stored in the squarer during C1 and C3 is acquired.

DC subtraction during period C4 would generate an error, as full subtraction was already applied during period C1. DC SUBTRACT is therefore turned off by transferring the source of Isub from the summing junction to Common 2.

Period C5

a. REF INTEGRATE opens, stopping the integrator action.

b. SAMPLE closure forces the squarer output to a hard zero, to nullify any leakage effects in the integrator switch.

c. REF SAMPLE closes to charge the sampling capacitor to the integrator capacitor voltage, by current from the integrator op-amp.

d. RMS Lo is switched from the Ref common 2C to the Sense SIG Lo in preparation for SIG squaring.

As the sampling capacitor changes its charge, its voltage-follower drives the voltage-to-current converter to change the DC subtraction current. During this period the new Isub is sourced from Common 2, but during the next SIG and REF integration periods, it will be subtracted from the squarer output current at the summing junction.

Periods C6 to CØ

As can be seen from Fig. 4.14.3, the closure pattern is repeated for SIG squaring, integration and sampling. The SIG circuit action is identical to REF, except that:

a. the squarer input is now the sensed sinewave;

b. the subtraction current has been set to a new value during period C5. This does not change again until period C5 of the next cycle;

c. During period CØ, the 'AC ERROR' output from the SIG sample-and-hold voltage follower is changed, updating the VCA gain via the error buffer and Error Amplifier.

d. RMS Lo was switched from the common 2C to SIG Lo during period C5 in preparation for SIG squaring. It remains connected to SIG Lo during the squaring periods C6, C7 and C8, and also during period C9 for the Sig integrator settling. At Period CØ it is reconnected to common 2C in preparation for REF squaring.

4.14.3.2 Comparator Action

The sequence described in 4.14.3.1 is necessarily simplified. When a new output demand changes the amplitude of the quasi-sinewave, a few sequence cycles are required to stabilize the conditions of the REF integrator, SIG integrator, subtraction current and AC ERROR OUTPUT. The circuit must also respond to demands for reduced output in addition to those for increases.

The comparator forms part of the output amplitude control loop, ultimately affecting the output voltage and hence the sensed voltage input to the squarer as 'SIG'. As the sequence recycles, the mean-square value of the SIG input sinewave will approach that of the REF quasi-sinewave, and as it does so the AC ERROR output must approach a steady-state value.

The squarer output current has an AC component in its waveform, but Isub being subtracted at the summing junction is a DC current. In the settled condition, Isub is driven on successive cycles to balance the quasi-sinewave REF^2 AC current (being applied to its integrator) about zero. The final level of Isub is just sufficient to be self-sustaining.

Meanwhile, the sensed SIG^2 current approaches the REF^2 value, and the same Isub is a DC analog of the quasi-sinewave mean-square voltage. In the output loop, the VCA is driven until the 4200 output (and sensed SIG input) is at the correct level just to generate a self-sustaining 'AC ERROR'.

In the comparator, Isub is subtracted from both SIG^2 and REF^2 currents. This maintains the AC AMPL ERROR as an analog of the difference between the quasi-sinewave and the output sinewave mean-square voltages (when the latter is reduced by sense conditioning to 1V Range levels). Thus when the sensed SIG input voltage approaches the quasi-sinewave REF voltage (mean-square values), the AC ERROR approaches stability and the system settles.

A further complication: a bias is applied to the squaring circuit to avoid distortion by maintaining permanent conduction. The bias is controlled by the value of the positive reference voltage, and a bias current is superimposed on the subtraction current. These factors will be discussed later during the circuit analysis.

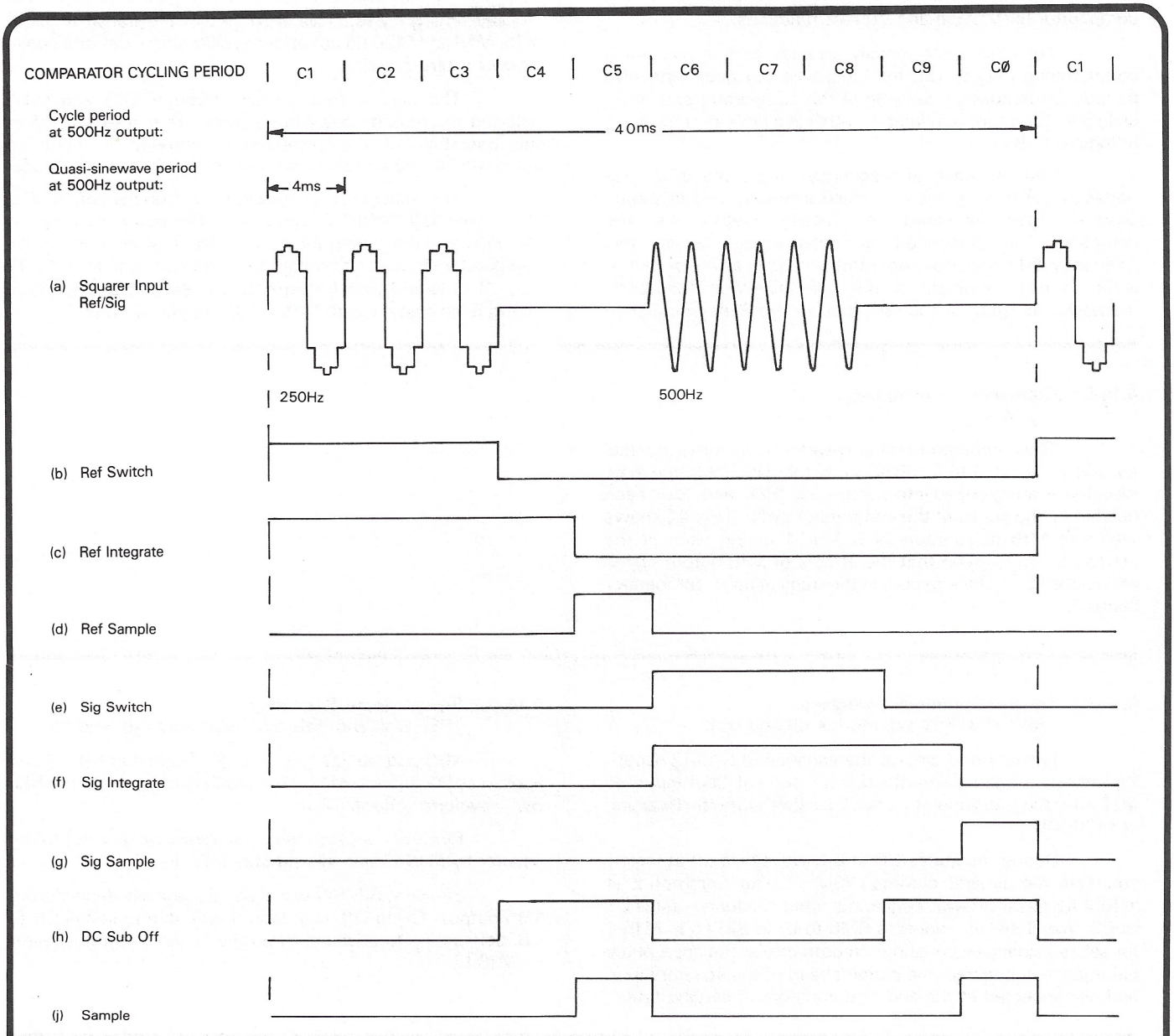


FIG. 4.14.4 SINE/QUASI-SINE COMPARATOR—SEQUENCE TIMING

4.14.4 Comparator Control Logic
(Circuit Diagram 430447 page 7.7-3)

TheComparator operating cycle originates at M15, which is a 10-bit sequencing counter, clocked at the quasi-sinewave frequency by the carry-out from M11-12.

The SYNCØ input to M15 RESET is a decoded address, whose function at logic-1 is to disable counters M11 and M15, inhibiting operation of the comparator and generation of the quasi-sinewave. In the 4200, SYNCØ is held permanently at logic-Ø, enabling both quasi-sinewave and comparator for Voltage and Current functions.

The clock continuously recycles M15 in ascending count through $Q_{Ø}$ to Q_9, ten clocks (ie ten quasi-sinewave periods) constituting one cycle of the comparator sequence. Only one 'Q' output is at logic-1 (+8V) at a time, the rest being at logic-Ø (−8V).

With increase of frequency range, the difference between the frequencies of sensed sinewave and reference quasi-sinewave increases in decade steps. As the comparison is performed at mean-square levels, this frequency difference does not matter, so long as the sinewave is at an exact multiple of the quasi-sinewave frequency. However, to optimize the operation of the Sense/Reference comparator, the zero crossings of the quasi-sinewave are synchronized to occur coinincident with a sinewave zero crossing, and all comparator state changes are also synchronized to sinewave zero-crossings.

Synchronization is achieved by clocking M17 so that all the analog switching data changes simultaneously. Thus data is latched from M17 'D' inputs to its permanently-enabled outputs, one complete quasi-sinewave period after it was clocked through M15. This ensures that the transit times of M15, M18 and M20 do not affect synchronism with the quasi-sinewave zero-crossing.

The data is thus strobed through M15 and M17, delaying the data by one clock period. This does not affect the operation of the comparator, although it must be accounted for when observing waveforms on an oscilloscope.

The sequence, as described in sub-section 4.14.3, starts with REF SWITCH connecting the quasi-sinewave to the squarer input during period C1. The logical origin of the comparator switch state during C1 corresponds to M15-2 (Q1 output) at logic-1; but because of the data delay its actual timing is coincident with M15-4 (Q2 output) at logic-1.

4.14.5 Comparator Timing Logic
(Fig. 4.14.5)

The comparator timing waveforms for the sequence are shown at Fig. 4.14.5. To illustrate the data delay, the main waveforms are grouped into two blocks: 'REF' and 'SIG', each headed by the states of the comparator cycle. Line (b) shows which of M15 (Q) outputs is at logic-1 during each of the states. It can be seen that the effects of M15 output states are delayed by 1 clock period, in the translation to comparator states.

4.14.5.1 Squarer Commons Switching
['REF' and 'SIG' waveforms (d) and (k)]

Waveform (c) shows the variation of M15-12 (Cout). Waveforms (d) and (k) are the direct results of Cout inputs to M17 after the translation by one clock shift (note the inversion at M20-10).

During the states CØ to C4, waveform (d) at logic-1 connects the squarer common (RMS Lo) to Common-2 at M16-4 for quasi-sinewave squaring; whereas during states C5 to C9, waveform (k) connects RMS to Lo to SIG Lo at M16-8 for sensed sinewave squaring. In both cases, the appropriate common is connected one period ahead of the squarer input, and disconnected at the end of the integrator settling time.

4.14.5.2 Squarer Input Switching
|'REF SW' and 'SIG SW' waveforms (e) and (l)|

M15 outputs Q1 to Q3 are 'OR' gated at M18-6 and applied as D2 input to M17. The result is to generate the REF SW waveform (e) at M17-7.

REF SW connects the quasi-sinewave as input to the squarer by M16-13 only during states C1 to C3.

Similarly, SIG SW waveform (l), logically derived from M15 outputs Q6 to Q8, is at logic-1 only during states C6 to C8, connecting the sensed sinewave as input to the squarer by M16-12.

4.14.5.3 Integration and Sample Switching

'INT' and 'SAMPLE' waveforms (f) and (h)

At any instant, the comparator is either sampling or integrating. The INT waveform is thus the inverse of the SAMPLE waveform.

SAMPLE

M15 outputs QØ and Q5 are 'OR' gated at M18-9 and applied as D3 input to M17. The result is to generate the SAMPLE waveform (h) at M17-10.

Therefore, CØ and C5 only, SAMPLE provides two enabling inputs to AND gates M13 at M13-2 and M13-5. It also places a hard zero on the squarer output by M7-5 (page 7.7-4) when this is disconnected from both integrator inputs. With both input and output at zero volts, any offsets are removed in preparation for the subsequent squaring and integration sequence.

INT

The 'SAMPLE' output of M18-9 is inverted at M20-4, applying logic-1 to the D1 input of M17 for the whole of the cycle except for CØ and C5. The INT output at M17-5 is waveform (f), which enables M13-1 and M13-13.

REF INT

INT is 'AND-gated' with REF waveform (d) at M13-11 to generate the 'REF INT' waveform (g), which is at logic-1 only during periods C1 to C4. During this time M7-12 (page 7.7-4) at logic-1 connects the squarer output to the REF Integrator input.

SIG INT

INT is 'AND-gated' with SIG waveform (k) at M13-10 to generate the 'SIG INT' waveform (m), which is at logic-1 only during periods C6 to C9. During this time M7-6 (page 7.7-4) at logic-1 connects the squarer output to the SIG Integrator input.

REF SAM

'SAMPLE' is 'AND-gated' with SIG waveform (k) at M13-4 to generate the 'REF SAM' waveform (j), which is at logic-1 only during state C5. During this time driver M6-1 (page 7.7-4) at logic-1 causes FET Q2 to conduct, connecting the REF Integrator output to the REF Sample-and-Hold input.

SIG SAM

'SAMPLE' is 'AND-gated' with REF waveform (d) at M13-3 to generate the 'SIG SAM' waveform (n), which is at logic-1 only during state CØ. During this time driver M6-7 (page 7.7-4) at logic-1 causes FET Q3 to conduct, connecting the SIG Integrator output to the SIG Sample-and-Hold input.

4.14.5.4 DC Subtraction

'DC SUBTRACT OFF' waveform (p)

Subtraction is required only when either input is being applied to the squarer. As REF SW and SIG SW already exist, it remains only to provide an OR function or join them. The analog circuits need an inverted waveform, so a NAND gate is used. For loading purposes two elements of M20 are connected in parallel: REF SW and SIG SW are combined as waveform (p) at M20-3 and M20-11.

Squarer Input Short

When at logic-1 during C4-C5 and C9-CØ, M7-13 places a hard short between RMS Hi to RMS Lo; otherwise the short is released.

Subtraction Current Control

During C1 to C3 and C6 to C8, DC SUBTRACT OFF at logic-Ø cuts off D8 (page 7.7-4), allowing Q6 to draw subtraction current through D6, D5 and R54. When at logic-1, D8 conducts and sets D5 and D6 in reverse bias, diverting the subtraction current.

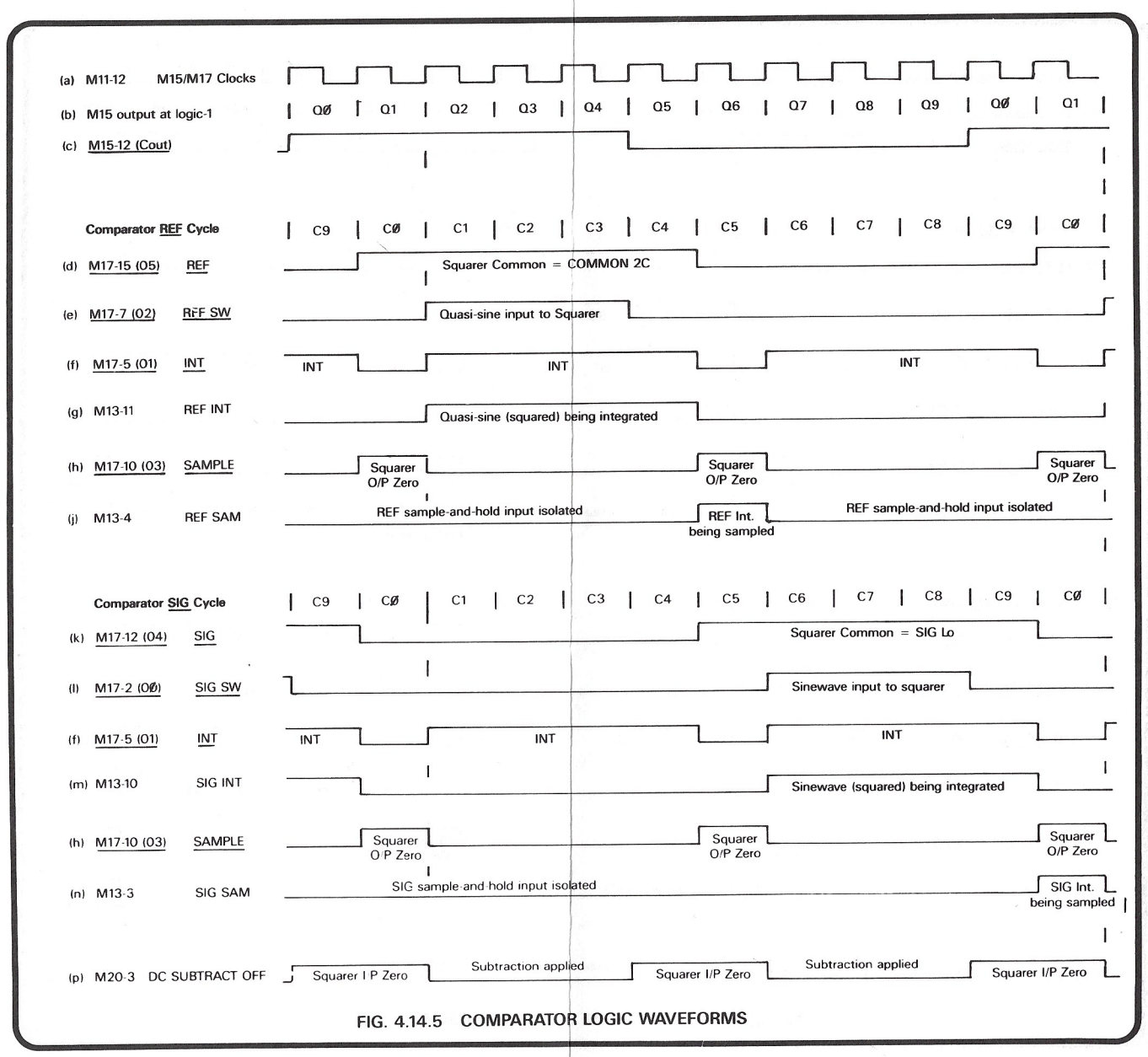


FIG. 4.14.5 COMPARATOR LOGIC WAVEFORMS

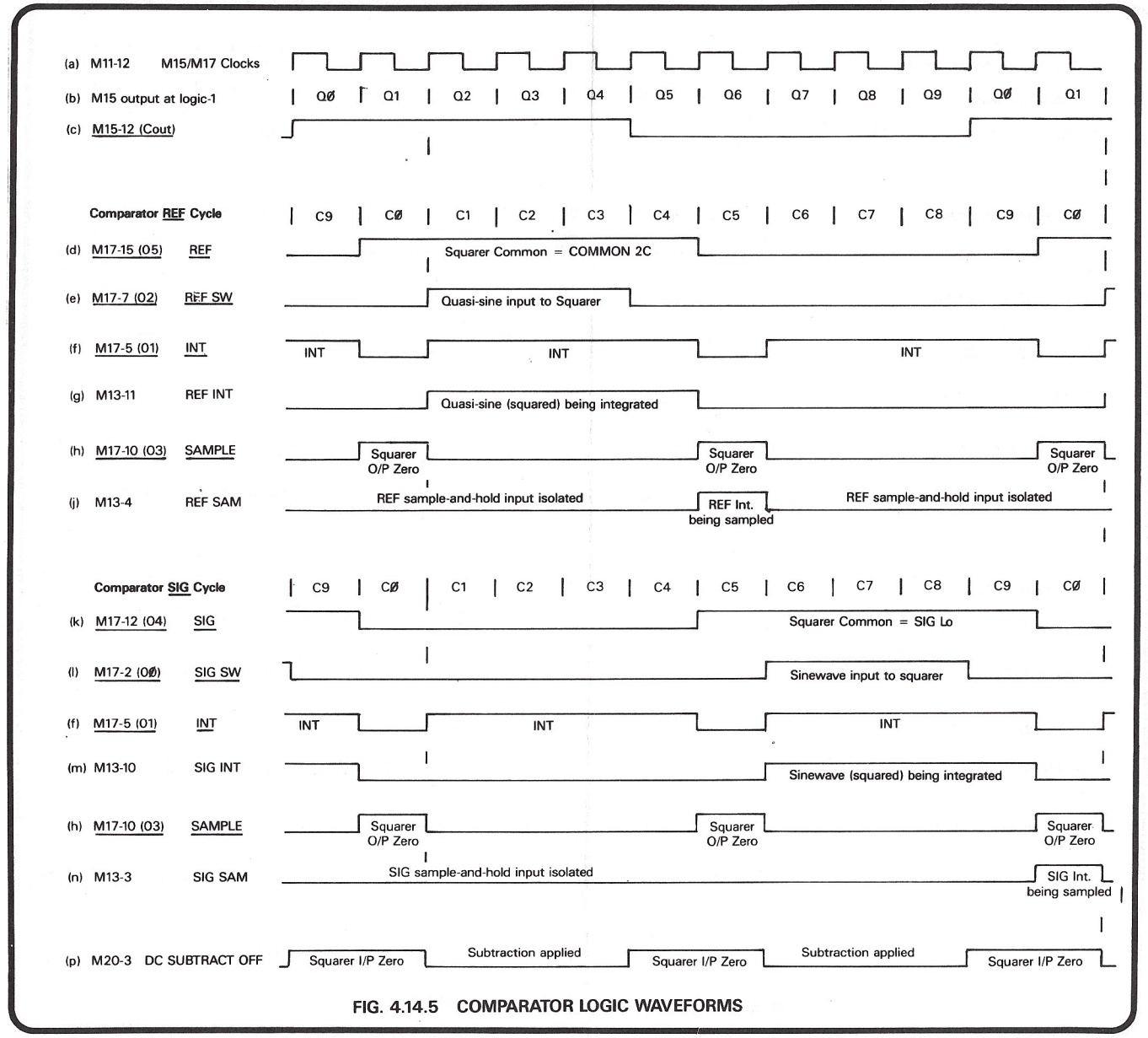


FIG. 4.14.5 COMPARATOR LOGIC WAVEFORMS

4.14.6 Square Law Detector Circuit
(Circuit Diagram 430447 Page 7.7-4)

The basic action of the squaring circuitry is the same as is used for $\sin^2$ and $\cos^2$ in the Sinewave Oscillator amplitude loop, but there are some differences in detail (Refer to Sect. 4.8.8).

The Square Detector is biassed in such a way that it is permanently turned on, to improve bandwidth and permit control of gain scaling. Its differential output current at AN3-3 and AN3-2 is proportional to the square of its input voltage divided by the bias voltage. The bias is derived from the DC version of the demanded signal level REF+ve, the DC output from the Reference Divider.

Thus the transfer proportionality of the signal magnitude is given by:

Vout α Vin^2/Vbias

but as Vbias is derived from REF+ve,

Vin/Vbias is a constant: k,

and the instantaneous squarer gain is:

$$\frac{d(Vout)}{d(Vin)} = \frac{d\left[\frac{kVin^2}{Vin}\right]}{d(Vin)} = 2k$$

Thus the basic gain equation has no amplitude or frequency components, so is constant over a wide bandwidth and dynamic range. The squarer therefore has a fast response at all signal levels.

The bias is applied as currents to Q17 and Q18 emitter circuits. The transistors in the array of M22 are all used as current generators.

4.14.6.1 Bias Control

The input to Reference Amplifier M24 is the positive DC REF+ve voltage, which varies between approx. 0.14V and 2.8V, depending on the output value selection.

M24 output voltage rises until M22-9 pulls enough current through R50 to reduce M24-3 to zero. The other transistors in M22 act as current mirrors, so their collector currents are defined by the REF+ve voltage and the resistance of R50.

Thus bias current is applied to Q17 and Q18 in direct proportion to the REF+ve voltage, which is an accurate analog of the demanded output value.

4.14.6.2 Current Driver

The 'SIG^2' and 'REF^2' current outputs from the square detector develop a differential voltage input between TP48 and TP49, to the current driver Q9/Q10/M19. This amplifier generates a single-ended current drive to the integrators.

Q9(B) collector drives the output directly, but in order to establish a stable DC voltage reference level, Q9(A) collector current is mirrored by Q10(B).

M19 bootstrap steers Q9(A) collector current through Q10(A), maintaining Common-2C potential at Q10(A) collector.

Q10(B) mirrors the Q9(A)/Q10(A) collector current so that when the differential input voltage between TP48 and TP49 is zero, Q9(B) collector current is all taken by Q10(B), and the potential at TP9 is the Common-2C zero, at high impedance.

Differential input variations between TP48 and TP49, due to 'SIG^2' and 'REF^2' outputs from the Square Detector are translated to differential currents into and out of the junction at TP9. The current difference passes through R35 and R148 during SIG INT states, and to R149 during REF INT states.

At other times, when the integrator input switches M7-8/9 and M7-11/10 are both open, the 'SAMPLE' waveform closes M7-4/3 to pass any difference current to Common-2C. (During the SAMPLE periods, DC SUBTRACT OFF is zeroing the Square Detector input RMS Hi anyway, by shorting to RMS Lo via M7-2/1.)

Resistors R35, R148 and R149 are of very low value compared with Q9(B) and Q10(B) output impedance, so the driver compliance is high.

4.14.6.3 Output Amplitude Loop —LF Gain Reduction

On the 100Hz Frequency range the gain around the output amplitude loop needs to be less than on other ranges. It is convenient to adjust the error immediately following its generation in the square detector, by shunting the input to the current driver.

Adjustment is in two stages, using dual open-collector comparator M21:

a. **For 100Hz Range selection**
The '100Hz' signal input to M21-3 is derived in the Frequency Synthesizer, and is at logic-1 when the 100Hz Range is selected by the operator. M21-1 is pulled up by R41 and Q7 conducts, connecting R43 and R44 between TP48 and TP49, thus shunting R49 and the base-emitter junctions of Q9. For a given 'SIG^2' or 'REF^2' signal, the input feed to the current driver is reduced.

b. **For frequency selections below 32Hz**
The '>31Hz' signal input to M21 is also generated in the Synthesizer.

i. For any frequency above 31Hz, the >31Hz signal is at logic-1, M21 output is at logic-Ø (−15V) and Q8 does not conduct.

ii. For frequencies of 31Hz and below, the >31Hz signal is at logic-Ø, M21 output is pulled up by R42. Q8 conducts, connecting R45 and R46 between TP48 and TP49, in addition to R43 and R44. For a given 'SIG^2' or 'REF^2' signal, the input feed to the current driver is further reduced.

4.14.7 Generation of the DC Subtraction Current

4.14.7.1 'REF' Integration

The integrator circuit is very basic. Feedback for M12 is by C25, but the input resistance is formed by R149, R35 and the output impedance of the Current Driver, which is heavily predominant. The current from the driver is virtually unaffected by R35 and R149.

M7-11/10 conducts for periods C1 to C4 (REF INT). During C1 to C3 the REF SW waveform inputs the quasi-sinewave to the squarer, and during C4 the squarer settles to its zero input.

The REF^2 output from the driver is an AC current, which for a constant quasi-sinewave amplitude is integrally charge-balanced about zero due to the DC subtraction, at twice the quasi-sinewave frequency. C25 therefore receives equal positive and negative charge during each cycle of quasi-sinewave, so the mean voltage at M12-1 does not change.

A discharge path for C25 is provided by Q5/R30. The 'INT HOLD' signal at J7-46 is at logic-1 when the 4200 is in 'OUTPUT OFF' condition, discharging both REF and SIG integrators. For so long as the 4200 output remains 'ON', the INT HOLD signal remains at logic-Ø, and the integrators are never discharged other than by the action of their inputs.

4.14.7.2 'REF' Sample-and-Hold

Q2 conducts during each 'REF SAM' period, when the charge on C25 has settled for the cycle. M12 drives C12 to the voltage on C25, and the voltage follower M4 passes the same voltage as 'REF ERROR' on to the REF V to I Converter.

Q2, C12 and M4 are low-leakage devices, and M4 input circuit is screened at low impedance to the sampled voltage. Thus the 'Droop' is specified as less than 20 microvolts during the 'Hold' part of the cycle when Q2 is not conducting.

4.14.7.3 REF V to I Converter

The circuit of M19 and Q6 converts the DC voltage output of M4 into the subtraction current. A second function is to draw an extra DC current which compensates for the bias control currents.

The DC 'REF ERROR' voltage from M4-6 is divided by R37/R31 and applied to the non-inverting input of M19. A second input results from the DC bias current drawn by M22-14, defined by the 'REF+ve' voltage and the two resistors AN2-10/7 and R141.

M19 drives FET Q6, which draws current via Q12-3 emitter, R54, D5 and D6. The current is sunk into Common-2C via R47, R38 and AN2-12/5, and into the −15V supply via the M22-14/12 bias circuit.

Capacitor C34 filters out any HF transients remaining from the REF SAMPLE switching edges, and D7 protects against positive excursions of Q6 gate.

In the simplified diagram of Fig. 4.14.2, the subtraction current is shown as being sourced by the summing junction. In reality, it is taken from Q12-3 emitter for three main reasons:

a. The Current Driver input bias is removed, allowing a zero-offset reference.

b. The control bias for the squarer is compensated at the earliest opportuity, reducing the required dynamic range of the driver.

c. Q12 emitter voltage remains virtually constant for all squarer inputs.

Relocating the subtraction point does not affect the essential action of the square detector and driver, because of the current-mirror action of the driver.

Subtraction is valid only during times when a quasi-sinewave or sensed sinewave is being input to the Square Detector. Thus for periods C1 to C3 and C6 to C8, diode D8 is held in reverse bias by the signal 'DC SUBTRACT OFF' at logic-Ø. During periods C4, C5, C9 and CØ, the signal is at logic-1, so D8 conducts and cuts off D5 and D6. The subtraction current passed by Q6 is then diverted through D8 from M20-11/3, the parallel 'DC SUBTRACT OFF' NOR gates' output being at logic-1 (page 7.7-3).

When an operator selects a different output value, the result is a change in amplitude of the quasi-sinewave. This unbalances the integrator input, so C25 charges to a different mean voltage at M12-1. The DC subtraction current change takes place over a few comparator cycles until balance is restored, when C25 and C12 will have charged to a new voltage.

4.14.8 'AC ERROR' Signal Generation

4.14.8.1 Integration and Sampling Circuit

The SIGNAL Integration and Sample-and-Hold circuitry is identical to the REF arrangement described in Section 4.14.7. Moreover, the SIGNAL Integrator M12 is the other half of a matched pair with the REF Integrator.

The difference lies in the timing. Switch M7-6 allows current to pass into the SIG integrator only during the periods C6 to C9, so it is the SIGNAL ($|\text{sensed sinewave}|^2$) current minus the ($|\text{DC REF}|^2$) subtraction current which is integrated.

The integrator voltage is sampled and output as the DC 'AC ERROR' voltage, into the output amplitude control loop (Section 4.9).

4.14.8.2 Output Amplitude Loop Action

Consider the case of 'OUTPUT OFF'

a. The quasi-sinewave has an amplitude determined by the 'OUTPUT' display value:

b. The quasi-sinewave is squared and appears as a current in R35 during periods C1-C4, but because Q5 is conducting, the REF integrator capacitor C25 is discharged. Thus the DC subtraction current is effectively zero (it is actually sufficient to cancel the DC current in R35 due to the squarer bias).

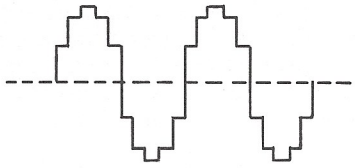
c. The AC ERROR signal voltage is zero, as Q5 conduction prevents any charge on the SIG integrator capacitor C26. Also, the output amplitude is zero, hence the sensed output applied to the squarer is zero.

Therefore during periods C6-C9 the current in R35 is zero.

Now consider the case when OUTPUT is switched ON, with the OUTPUT display set to the minimum value of 9% of range:

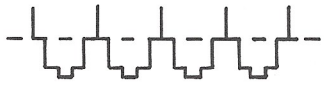
As the quasi-sinewave is already present, it is squared into a negative-going waveform in R35.

Quasi-Sinewave Input



During the first comparator cycle, this appears as a voltage at TP9 thus:

$(\text{Quasi-Sinewave})^2$
Zero Reference



The standing bias on the Ref. V to I Converter has immediately set the $(\text{quasi-sinewave})^2$ to an approximate zero mean.

The $(\text{quasi-sinewave})^2$ current is integrated across C25, resulting in a positive 'REF ERROR' voltage after period C5, and hence a positive subtraction current in R35. The effect of the current can be seen in the TP9 voltage waveform: an increase of $(\text{quasi-sinewve})^2$ amplitude is accompanied by a positive shift as its mean value seeks coincidence with zero.

After a few comparator cycles the current in R35 becomes charge-balanced about zero, the DC subtraction current stabilizing to a steady-state value.

Meanwhile, during the 'SIG' sections of the comparator cycle, the positive subtraction current is integrated across C26. A negative 'AC ERROR' voltage is generated, which increases the 4200 output voltage via the VCA. This increase is detected by the sense feedback circuits. After squaring, the result is an AC current in R35, whose mean level begins to offset the effect of the subtraction current on the SIG integrator.

After a few comparator cycles, the AC SIG^2 mean current and the DC subtraction current are equal and opposite, so the current fed through R35 into the integrator is charge-balanced about zero. The itegrator capacitor C26 is thus being charged and discharged by the same amount during each half-cycle of output (SIG^2 current being at twice the output frequency), and so the AC ERROR voltage stabilizes.

Fig. 4.14.6 illustrates three stages in the process of increasing output from zero; observing the current in R35 (ie. the voltage at TP9), the 'AC ERROR' signal, and the output sinewave. The waveforms are not to scale.

Stage 1. This is the first cycle that the quasi-sinewave starts to charge C25. During period C6 a non-zero subtraction current is applied to the SIG integrator, resulting in a non-zero value of 'AC ERROR', starting at CØ as the integrator voltage is sampled. This causes the 4200 sinewave output to rise from zero.

Stage 2. On the next cycle the subtraction current imposes a positive shift on the R35 waveform during C1-C3 and C6-C8. The squared quasi-sinewave does not change in amplitude, but it is more equally balanced about zero, so the next increase in subtraction current will not be so great.

During C6-C8 the sinewave is being applied to the squarer, so TP9 exhibits its squared waveform shifted positively by the subtraction current. A smaller increase in 'AC ERROR' and output sinewave results, as the AC input to the SIG integrator is more equally balanced about zero.

Stage 3. In this state the loop has stabilized. The squared quasi-sinewave and sensed sinewave are both charge-balanced about zero, the subtraction current and 'AC ERROR' have reached constant values, and the 4200 output is stable.

4.14.8.3 'AC ERROR' V-to-I Converter

(Circuit Diagram 430447 page 7.7-6)

To avoid pick-up during transit, the AC ERROR voltage is converted into a current, for transmission to the Error Amplifier on the Sine-Source Assembly. One half of M3 is used as a unity-gain inverting buffer, and the other as a voltage-to-current converter. The relay RL1 is not fitted, so M3-7 is linked directly to the test switch S1 'NORM' terminal.

At M3-7 the DC 'AC ERROR' voltage is inverted and used to drive the current converter via AN1-3/12. The current in AN1-4/13 is mirrored by the current in AN1-11/6 (AC AMPL ERROR), which is sourced in the Sine-Source Assembly by M41a, the Error Amplifier (Circuit Diagram 430446 page 7.6-3).

As the AC ERROR signal DC voltage is varied by the comparator, the current in M41a input resistance also varies, and is converted into a varying voltage at M41a-1. This voltage is used to control the main voltage-controlled amplifier M48 via Q71.

For further information refer to Section 4.10.

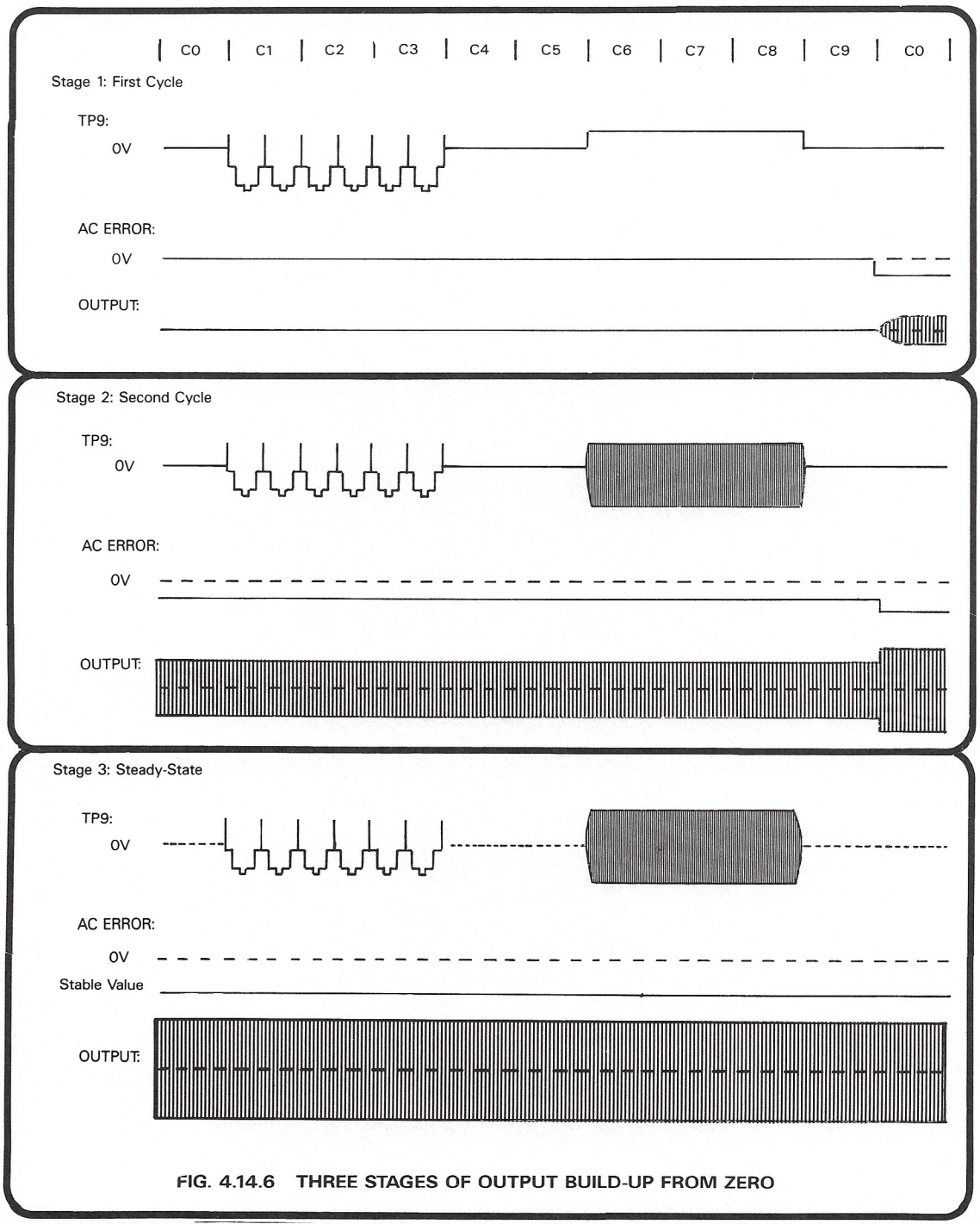


FIG. 4.14.6 THREE STAGES OF OUTPUT BUILD-UP FROM ZERO

The circuits described in this section perform the following functions:

(1) Convert the ACI Reference Voltage into a reference current, having a high-impedance source.
(2) Generate output currents whose value varies directly as the value of the ACI REF voltage.
(3) Provide switching of the AC Current Output and Range, under the control of the Analog Control Interface.
(4) Sense excess output (compliance) voltage, providing a $\overline{\text{LIM ST 1}}$ status signal to the CPU via the Analog Control Interface.

The voltage-to-current converter is located on the Current assembly, providing five ranges of current output. The output is drawn from the 4200 I+ and I− terminals; the Hi and Lo terminals not being used. The five ranges are 1A, 100mA. 10mA, 1mA and 100μA, each extending to 100% overrange.

The output currents are controlled within each range by the value and frequency of the ACI(REF) voltage. This reference voltage is generated by the circuitry used for voltage ranges: the 1V range for the 100μA and 1A ranges; the 10V range for the 1mA, and 100mA ranges. The highest frequency available is 5kHz.

4.15.1 Basic Voltage-to-Current Converter

The basic arrangement is shown in Fig. 4.15.1. A variable AC reference voltage is developed across R1 between the output and the inverting input of the high-gain operational amplifier. The non-inverting input is connected to the output by a resistor network, part or all of wich is current carrying.

With both positive and negative feedback the amplifier forces its differential input to zero. It can only do this by adjusting the current in the current-carrying part of the positive feedback path until the full value of the reference is developed across the path. For example in Fig. 4.15.1 no current flows in R2, so all of VRef is developed across Rs.

The values of VRef and 'shunt' Rs thus determine the value of current flowing in the external circuit. In the 4200 the values of Rs are switched to select the range in use, and VRef is adjusted to vary the output current within the selected range.

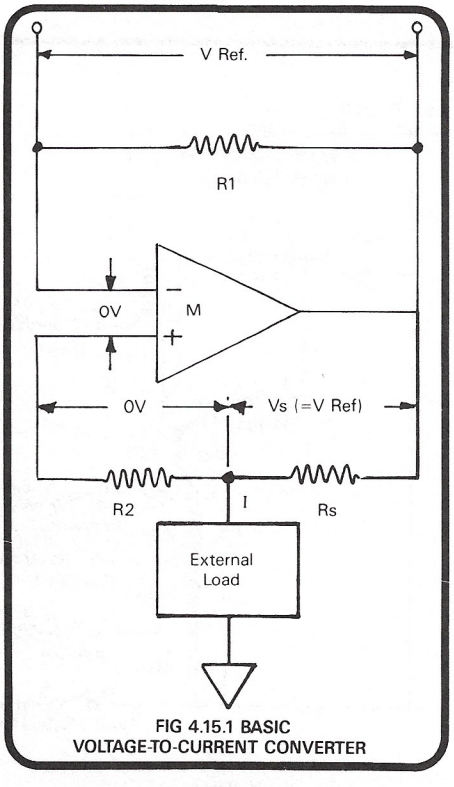


FIG 4.15.1 BASIC VOLTAGE-TO-CURRENT CONVERTER

4.15.2 Two-stage Current Generator

(Circuit Diagrams 430555 Page 7.8-1 and 430540 Page 7.13-3)

Because an 'I−' terminal is necessary to provide a return path for the output current, a 'compliance' signal voltage will be generated at the output terminal 'I+' with respect to I−. The magnitude of the compliance voltage is specified in the User's Handbook. This specification is met by employing a two-stage circuit.

A fixed voltage-to-current conversion stage is followed by a range-switchable current amplifier. The combination is simplified at Fig. 4.15.2.

The AC Reference voltage is applied via two resistors R1 and R3 to both inputs of the first stage. It is arranged for the resistor values to conform to:

$$\frac{R2}{R1} = \frac{R4}{R3},$$

so the output impedance of the stage is virtually infinite, and its output 'floats'.

The second stage is a current amplifier, receiving the output current of the fixed stage to generate a voltage across R5. This voltage is repeated across R6, whose value is range-switched. Any resistor Rs does not affect the output, as it carries no current. Bootstrap supplies are used for the current amplifier, to improve common mode rejection.

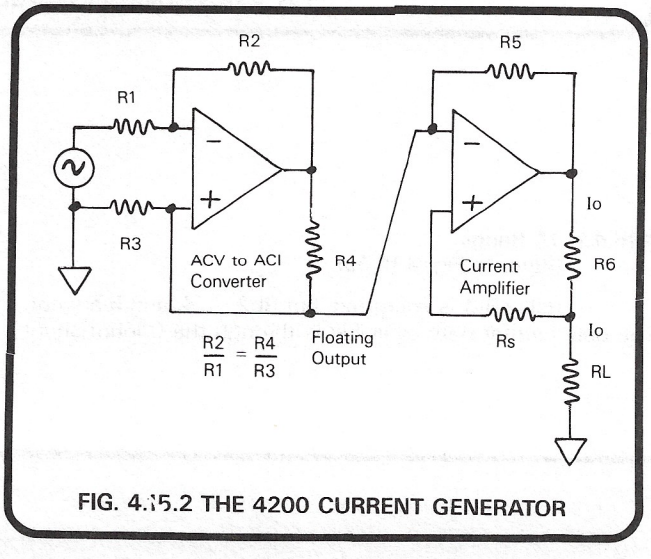


FIG. 4.15.2 THE 4200 CURRENT GENERATOR

4.15.3 Current Reference 'PHI (ACI REF)'
(Circuit Diagram 430447 Page 7.7-1)

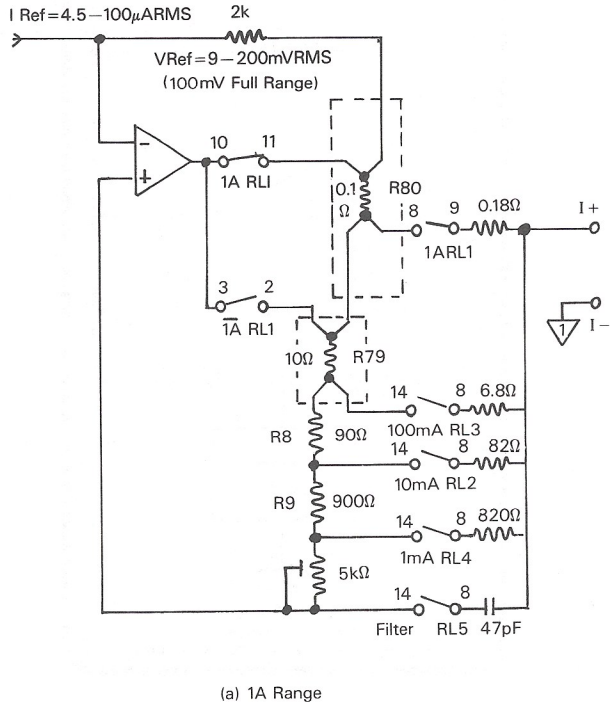
On the 100μA and 1A ranges, the 1V range circuitry provides the 2V RMS Full Scale reference voltage; but on the 1mA, 10mA and 100mA ranges the 10V circuitry provides 20V RMS at Full Scale.

On the AC assembly, when the 'I' function is selected, relay RL29 is energized and RL10 is not. The reference voltage for the current generator is derived from PHI (ACV) and PLO (ACV) signals; and sensed at the input to the Current assembly. The sensed ACI REF is returned to the appropriate connections of the 1V/10V Sense Amplifier. The 4-wire connections are made via J7, pins 69 to 71, to the same pins of J8 on the Current assembly.

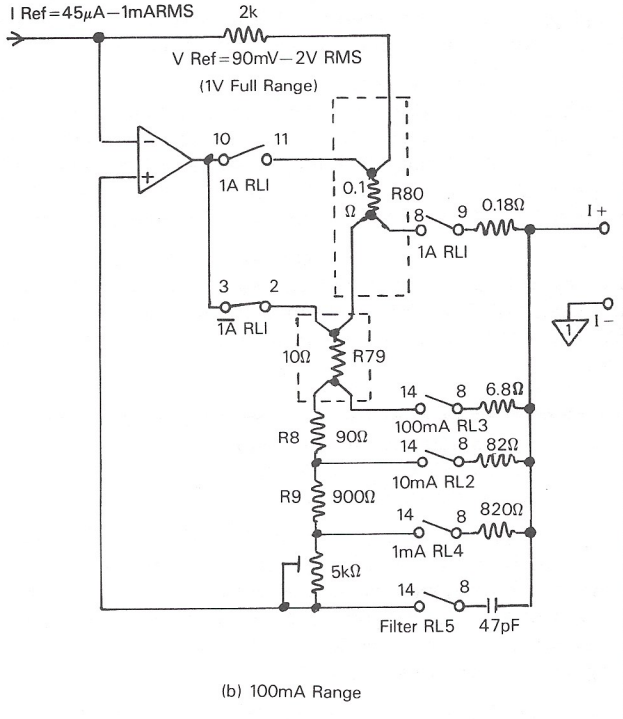
4.15.4 Range Selection

Fig. 4.15.3 shows two Range configurations of the current amplifier. In each case VRef is 10% of the ACI REF voltage. RL1 is a bistable latching relay, in which solenoid current is required only to change state.

In the 4200, the voltage across the I+ and I− terminals is allowed to rise to 3V RMS with full compliance. Each range incorporates a series resistive element connecting the range selection relay contact to the I+ terminal. These resistors enhance the stability of the circuit, with reactive loads.



(a) 1A Range



(b) 100mA Range

FIG. 4.15.3 CURRENT RANGE CONFIGURATIONS

4.15.4.1 1A Range
(Refer to Fig. 4.15.3a)

Relay RL1 is energized, but RL2, 3, 4, and 5 are not. The only current path available is through the 0.1ohm shunt R80. As VRef is scaled to 100mV RMS Full Range, the full range current in the shunt must be:

$$\frac{100\text{mV}}{0.1\text{ohm}} = 1\text{A}.$$

4.15.4.2 100mA, 10mA, amd 1mA Ranges

(Refer to Fig. 4.15.3b)

Relay RL1 is un-energized, contact RL1-3/2 is closed, contacts RL1-10/11 and 8/9 are open. One relay from RL2, 3 and 4 is energized by range, RL5 is also energized on the 10mA and 100mA ranges for extra HF filtering. All currents now avoid the 0.1ohm shunt, passing instead through the 10ohm shunt R79.

R79 is mounted with R80 on a separate heatsink assembly, plugged into the main Current assembly (refer to the Layout Drawing, page 7.8-1 for alternative versions).

On the 100mA range, VRef is scaled to 1V RMS Full Range, so the full range current flowing through R79 to the I+ terminal via RL3-14/8 must be:

$$\frac{1V}{10ohms} = 100mA.$$

For the 10mA range, R8 (90.00ohms) is included in the current path, so the full range output current is reduced to 10mA. 900ohms (R9) is added on the 1mA range.

4.15.4.3 100μA Range

(Refer to Fig. 4.15.3b)

The hardware is switched as for the 1mA range, but the ACI REF voltage is obtained, as for the 1A range, from the 1V range circuitry. Thus VRef is scaled to 100mA RMS Full Range, and the full range output current is 100μA.

4.15.5 Voltage-to-Current Converter

(Circuit Diagram 430555 Page 7.8-1)

The reference voltage PHI (ACI REF) is applied to the inverting input of M8 via resistor R45A, with R45B as feedback resistor. Similarly R46A and R46B are connected on the non-inverting side. The 18Mohm resistors R82 and R83 shunt R46A to allow compliance adjustment by R51. R86 refers the input to Common-I1, the main 'signal' common.

4.15.5.1 Feed to the Current Amplifier

The output current from the converter, flowing through R46B to restore M8 input virtual-common, passes via R85 into the Current Amplifier feedback resistor R43. It generates a reference voltage between the output of the whole Current Amplifier and its inverting input. This is reflected on its non-inverting side by the current flowing through the range-switched output 'shunts'.

4.15.6 Voltage Preamplifier

M3, M4 and Q6 form a high-gain, chopper-stabilized voltage amplifier. The input offset of Q6 is trimmed by M3, itself a chopper-stabilized amplifier of high gain and approximately 10Hz bandwidth. Q6 provides the bandwidth necessary to pass the signal frequencies and reject common-mode noise.

M4 contributes additional gain and drives the high-current output stage via link TLE. Its load, consisting of R26, R23 and R28 shunted by Q7 in the Heatsink assembly, is supplied with a constant current by Q9, D6 and Q11. Additional frequency compensation is provided by C43 and R81.

The supplies to Q6 and M3 are bootstrapped by M7 for common-mode rejection, also linearizing the preamplifier's dynamic response. Extensive screening and filtering is employed to eliminate the effects of the chopping spikes at the inputs and output of M3.

4.15.7 High Current Output Stage

(Circuit Diagrams 430555 Page 7.8-1 and 430540 Page 7.13-3)

The main current amplifier and temperature-sensing driver load (Q7) are located on the PS/I Heatsink assembly. The quiescent current 'SET IQ' adjustment is situated on the Current assembly.

4.15.7.1 Temperature Compensation

Transistor Q7, in parallel with R26, R23 and R28 on the Current assembly, acts as the load for the preamp. buffer. As the heatsink temperature increases, Q7 conduction increases, reducing the drive to the current amplifier. This compensates for increased intrinsic quiescent current in the two Darlington output devices.

4.15.7.2 Quiescent Current Adjustment

FET Q9 acts as constant 1.4mA ballast for the 3.3V zener diode D6, which sets the voltage across R27 to approx. 2.6V. This establishes a constant current in the buffer load.

The voltage across the load is supplied to the PS/I heatsink as drive for the high-current amplifier. The tapping at J8-110 sets the base conduction level of Q7 on the heatsink, which in turn sets the level of its collector conduction, adjustable by R23. This adjusts the quiescent current in the output devices Q1 and Q2.

4.15.7.3 Current Amplifier

Darlington emitter-followers Q1 and Q2 form the current output amplifier, current-limited by Q5 and Q6. The bias is set to provide some 100mA of quiescent current, which reduces the output resistance of the stage, improving the dynamic response of the output current. This also suppresses any tendency for the drive from the preamp. buffer to fluctuate for output currents around zero; as the drive voltage must slew through approximately 1.3V after switching one device off before the other is switched on.

The current shunts complete the feedback and output circuits as described in paras 4.15.1 and 4.15.4, the output current being fed to the I+ terminal via protection circuitry and output switching.

4.15.8 Output Protection

Diodes D18 and D19 are 5V, 5Watt zeners, placing an absolute limit on the excursions of output voltage. The output compliance specification is valid only up to 3V RMS across the output terminals. Nevertheless, occasions may arise when a user overloads the circuit by attempting to drive current into open circuit (e.g. by disconnecting from a load with OUTPUT ON). In this case D18 and D19 protect any voltage-sensitive load by limiting the output voltage to 5V. But before the voltage reaches this limit, the overload protection circuit generates the $\overline{\text{LIM ST 1}}$ signal.

4.15.8.1 Guard Buffers

M1 guards out the leakage of D18 and D19 in normal operation, and protects against other leakage, by maintaining the output screens and shields around the output circuitry at the output potential.

In addition to its bootstrap function, M7 also acts as a buffer for guards around the amplifier input, thus preventing any common-mode disturbances from affecting the performance of the main amplifier.

4.15.8.2 Overvoltage Detection

The output guard buffer M1 drives the overvoltage detection circuit. M15 divides the output voltage by two and acts as an inverting full-wave rectifier, accommodating both polarities. The full-wave rectified voltage at M15-14 thus increases negatively as the AC output increases, charging C32 to its mean value at M15-10. M15-9 is biassed to −2.2V, so M15-8 reverse biasses D10 unless the terminal voltage exceeds 4.8V RMS, when M15-8 swings the negative rail and pulls the $\overline{\text{LIM ST 1}}$ line to −15V (logic-Ø).

The diode D10 is part of a diode-OR gate, linking $\overline{\text{LIM ST 1}}$ to the $\overline{\text{LIM ST}}$ line, which enters the Reference Divider at J4-76. The CPU receives the $\overline{\text{LIM ST}}$ status signal via the SSDA serial interface, and if at logic-Ø presents the 'Error OL' message on the MODE display. If in the 100mA or 1A range, the 4200 Output is turned off and the DC precision reference is ramped to zero, to limit the power developed as heat within the instrument.

4.15.8.3 Current Switching Logic

(Circuit Diagram 430555 Page 7.8-2)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' output in the Serial/Parrallel Data Converter. Offset positive logic is used:

logic-Ø = −15V, logic-1 = 0V.

The signals enter the Current assembly via J8 from the Mother assembly.

M12 and M14 are Darlington open-collector inverting drivers. The relay drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (−15V) on those not required. A selected driver operates its relay by pulling its output to −14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J8-60 is pulsed to logic-Ø for 50ms. Q1 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD (IG)}}$ pulse has ended they are held on by the 13.3V between −0.7V at the cathode of D1 and −14V at the selected driver output. This method reduces the local heat, generated by energized relay solenoids, in the relay contacts.

RL1 is a bistable latching relay with two operating solenoids. A logic-Ø at pin 6 switches the 1A range on, and at pin 1 switches it off. Normally both pins are floating on open collectors, so the relay remains latched on in one bistable state with both solenoids un-energized. During the 50ms $\overline{\text{UPD (IG)}}$ pulse, M16-1 and M16-12 are enabled, allowing the 1A range switching-logic state to change RL1 over (if required), before the $\overline{\text{UPD (IG)}}$ pulse ends.

4.15.8.4 Range Switching

Range control data is input as a 3-bit code on IRØ, IR1 and IR2 lines. The bit-pattern is decoded to '1 of 8' by M6, to energize the correct relays for the selected range. In the 4200, only five of the M6 'Q' outputs are connected (Links LKQ and LKS are broken). The resulting variants are listed in table 4.15.1 against range selections.

4.15.8.5 Current Zero-Output

For zero output, the lines from the current generator to the I+ and I− terminals are disconnected. The 'OFF' signal is set to logic-1, and the $IR_{2-Ø}$ code is '0,0,0'. This sets all M6 outputs to logic-Ø, so RL1 latches in the $\overline{\text{1A}}$ position (R79 is selected in preference to R80). Relays RL8 and RL9 are de-energized by the OFF signal, to disconnect the output from the I+ and I− terminals, and short it to the current common-I1.

The Current Range relays RLs 2, 3 and 4, and the filter relay RL5, are all un-energized. While setting OFF to logic-1, the CPU also forces the Precision DC Reference to ramp down to zero, so the ACI REF voltage also falls to zero, and the current generator has no input. Thus the high current amplifier is not trying to produce an output current, and will not be damaged.

4.15.8.6 Function Switching

When the Current function is deselected, this means that the Voltage function is selected. The $\overline{\text{I FNCT}}$ signal is set to logic-1 to energize relay RL23, which connects the voltage output lines to the front panel terminals.

The $IR_{2-\emptyset}$ code is '1,1,1', setting only M6 'Q7' output to logic-1 (pin 4). Thus the range relays RLs 2, 3 and 4 are all un-energized. Relays RL8 and RL9 are un-energized, disconnecting the current output and shorting it to the current common-I1. RL1 is latched in the $\overline{1A}$ position, selecting R79 in preference to R80; and RL5 connects the 10mA/100mA filter.

In the AC assembly (Circuit Diagram 430447 pages 7.7-1 and 7.7-5), the $\overline{\text{I FNCT}}$ signal (J7-86) at logic-1 de-energizes RL9. This disconnects the ACI REF lines (J7-69 to J7-72) from the ACV lines. Thus the voltage to current converter (M8 on the Current assembly) receives no input voltage, and so no current is generated.

4.15.8.7 'BARK DELAYED'

The 'BARK' signal does not affect the Current assembly relays. However, if the Watchdog is activated, all outputs from the Control Data latches in the Reference Divider are 'Tristated' by the 'BARK DELAYED' signal. This allows the pull-up resistors (AN1) and pull-down resistor R84 to become effective. Thus the lowest current range is selected and current output is cut off.

4.15.8.8 $\overline{\text{I ST}}$

The $\overline{\text{I ST}}$ line at J8-98 is pulled down to −15V (logic-Ø) for as long as the Current assembly is fitted in the instrument. This state is passed back via the Reference Divider (J4-68) and the SSDA serial link to the CPU (Circuit Diagram 430535 page 5). Thus the CPU recognizes that option 30 is fitted, and can operate the appropriate programs.

Function	Range	Range Code $IR_{2-\emptyset}$			M6 Output Pins					Signals		Relays Energized						
					Q2	Q3	Q4	Q5	Q7			RL1	RL2	RL3	RL4	RL5	RL8 RL9	RL23
		IR_2	IR_1	$IR_\emptyset$	2	15	1	6	4	OFF	$\overline{\text{I FNCT}}$	6/7 1/12						
ACV/ON	N/A	1	1	1					1		1	*				*		*
ACI/ON	100μA	1	0	1				1				*			*		*	
	1mA	1	0	1				1				*			*		*	
	10mA	1	0	0			1					*	*			*	*	
	100mA	0	1	1		1						*		*		*	*	
	1A	0	1	0	1							*				*	*	
ACI ZERO	Any	0	0	0						1		*						
'BARK DELAYED'	Any	1	0	1				1		1	1	*			*			*

Table 4.15.1 Current Assembly Switching Logic

4.16 POWER SUPPLIES

The circuits described in this section perform the following functions:

(1) Line power switching, fusing, filtering, voltage selection and transformation.

(2) Main digital supply generation and distribution (Outguard)

(3) Display high voltage supply generation.

(4) In-guard stabilized supply generation for Common-2 and Common-4 circuitry.

A simplified power-distribution block diagram appears at Fig. 4.16.1.

The power input module is mounted on the rear panel. The mains (line) transformer is located in the rear section of the instrument, close to the In-guard and Out-guard Power Supply assemblies. (For details of location and attachment, refer to Section 3; and Section 7, page 7.0-1).

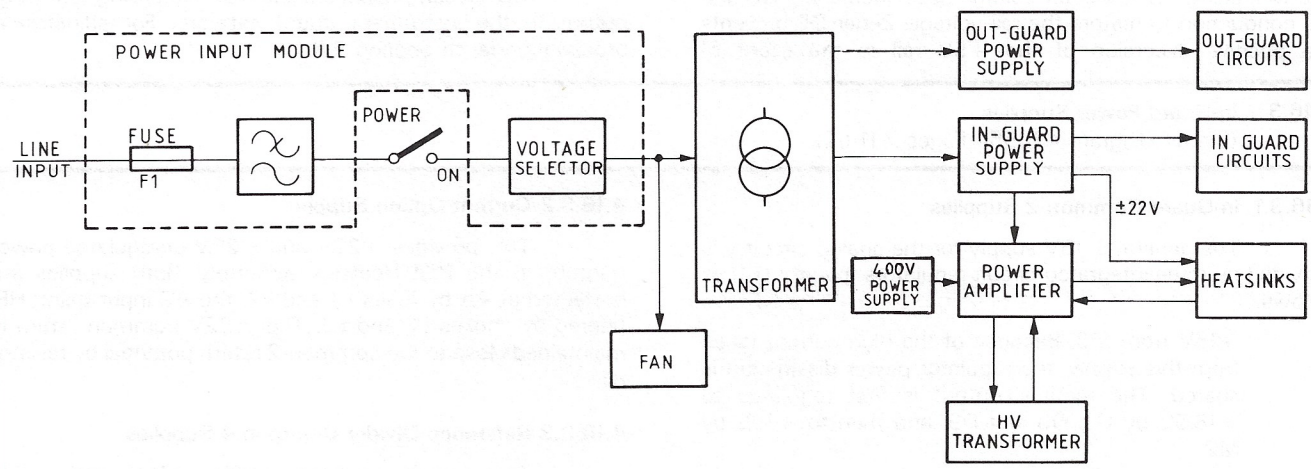


FIG. 4.16.1 POWER DISTRIBUTION BLOCK DIAGRAM

4.16.1 Line Power Distribution (Fig.4.16.1)
(Circuit Diagram 430439 Page 7.17-2)

The single phase line supply enters the 4200 via a 3-pole input cable at the rear of the instrument. The cable connector plugs into a power input module which contains a fuse, filter and line voltage selector pcb. (For details of fuse values and operating voltage selection refer to the User's handbook, Section 2).

Both 'line' and 'neutral' rails are filtered by a low-pass LC network before being fed through the instrument to the two-pole 'Power' switch on the front panel.

The switched supply is fed back to the power input module, to the voltage selector pcb, which configures the line transformer primary circuit as determined by the user. Power for the air circulation fan is provided directly from the power input module.

All line transformer secondaries are electrostatically decoupled from the primaries by a ground screen between the windings. The secondaries which supply the Common-2 and Common-4 in-guard circuits are decoupled by an additional screen which is connected to the instrument guard.

4.16.2 Out-Guard Power Supplies
(Circuit Diagram 430561 Page 7.10-1)

4.16.2.1 Digital Main Supply

This circuit provides:

(1) +8V unregulated supply for use in the Front and Digital assemblies.

(2) +5V regulated supply for out-guard digital circuits.

4.16.2.2 +8V Unregulated Supply

This is taken directly from full-wave rectifier D1, D2 via fuse F1 (rated at 4A).

4.16.2.3 +5V Regulated Supply

The output voltage is controlled by series regulator Q5, Q6. Load current is sensed by R1 in the base-emitter circuit of Q1, which increases the conduction of Q5 and Q6 parallel combination for increases of load current. The 2.45V zener D4 provides the reference voltage for comparator M1 at M1-3. The output voltage is sensed between the +5V and DIG common rails on the Mother assembly, and divided down to reference potential at M1-2. R8 and R9 ensure that regulation persists even if the sense links are disconnected.

M1 output drives Q2 whose collector voltage controls Q5 and Q6 conduction. If the +5V rail voltage falls due to loading, Q2 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage. Zener D5 prevents the positive excursion of the +5V rail in the event of regulation breakdown. Zener D3 restricts positive excursions of Q2 base voltage, and hence the drive to Q5 and Q6, to provide current limiting. C9 and C10 give a controlled fast response to reduce the effects of transients on the +5V rail.

PTC thermistor R7 protects the power supply from high ground-leakage currents, notably in the external circuits of the IEEE 488 bus system. R7 presents a minimum of 80ohms between the digital common line and ground; this resistance increasing with increasing current.

4.16.2.4 −180V Display Supply

180 Volts are required to operate the digital plasma displays on the Front assembly. Because the display anode drivers are powered from the Digital Main Supply +5V rail, the 180V positive pole is referred to this rail in the power supply. The display cathode is therefore at a potential of −175V. Refer to Section 4.4 for further details.

Series regulation is provided by D6, R16 and Q3; and shunt regulation by D7 and Q4. A supplementary +5V supply is fed out to the front assembly from J4-21. This is available to power the LEDs in the front panel keys, but is not used on the 4200.

4.16.2.5 Common Mode Null

This circuit provides a line-hum cancelling (bucking) output to the instrument guard network. For adjustment procedure refer to Section 5.8.

4.16.3 In-Guard Power Supplies
(Circuit Diagram 430554 Pages 7.11-1/2)

4.16.3.1 In-Guard Common-2 Supplies

The general ±15V supply for the analog circuitry is provided by three integrated-circuit regulators (page 7.11-1) as follows:

+15V from M2. Because of the high current taken from this supply, the regulator power dissipation is shared. The rectifier output is first regulated to +18.5V by Q1, Q3 and D9; and then to +15V by M2.

−15V from M1. This is a mirror image of the positive supply.

−10V from M6, derived from the −15V supply.

The supply is protected by 3.15A fuses F3 and F4 at the bridge rectifier output. Chokes L4 and L5 attenuate HF transients on the AC input.

The ±8V supply for the Sine-Source assembly is provided by two integrated-circuit regulators M8 and M9 (page 7.11-2). The supply is protected by 1A fuses F5 and F6 at the bridge rectifier output. Chokes L7 and L9 attenuate HF transients on the AC input.

4.16.3.2 Current Option Supply

This provides +22V and −22V unregulated power outputs to the PS/I Heatsink assembly. Both supplies are protected at 4A by fuses F1 and F2, the AC input being HF-filtered by chokes L2 and L3. The ±22V common return is maintained close to the common-2 return potential by resistor R1.

4.16.3.3 Reference Divider Common-4 Supplies

This circuit provides +36V, +15V and −15V regulated outputs to the Reference Divider in-guard circuits. The +36V supply is also used to power the +20V Master DC Reference.

Two secondary windings of the line transformer are used, and inter-supply transients are reduced by the special coupling arrangements of common-mode choke L10. The rectified output from bridge W4 is series-regulated by M3 to produce the +36V supply. R2/R3 sense the output voltage.

D11 and M4 reduce the +36V to generate the +15V regulated supply.

The −15V supply is provided by bridge W3 and regulator M7.

4.16.3.4 ± 38V Common-2 Supply

(Circuit Diagrams 430532 Page 7.16-5 and 430544 Page 7.12-1)

The ± 38V regulated supply is solely used to power the 10V Amplifier in the Power Amplifier assembly. It is plugged into the Mother assembly in the rear compartment next to the Heatsinks.

The mains (line) transformer 40VRMS secondary centre tap is referred to Common-2 on the Mother assembly. It provides a variable AC output by R25 on the Mother assembly to balance line-induced voltages on the guard screens. The 40V is rectified, filtered and smoothed on the Mother assembly before being passed to the regulator at approximately ± 50V DC.

On the 38V Supply assembly the output voltage is controlled by series regulators Q2 and Q1. As the regulator is symmetrical, only the positive side is described.

The output voltage is divided by R26 and R25 to provide a sense signal for comparator M1, which is powered by a local shunt regulator D8/R16/C8. The 2.45V reference for the comparator is derived by D6/R23 from the comparator supply.

M1 output drives Q8 whose collector voltage controls Q6 and hence Q2 conduction. If the +38V rail voltage falls due to loading, Q8 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage.

Load current is sensed by R24 in the base-emitter circuit of Q5, which is normally cut off unless the load current exceeds 170mA. At this point Q5 conducts and pulls down the base of Q6, setting a hard current limit.

Zener diode D2 turns Q5 hard on in the event of an output short circuit, providing a rapid response to catastrophic failure in the 10V power amplifier circuitry. As the output voltage falls below +22V, D2 arrests the fall on Q5 base, switching Q5 hard on and tuning Q6 and Q2 off. This leaves D2, R8 and R9 controlling the output current, which falls to less than 500μA.

When the load is removed, the conduction of Q5 via R26/R25 is insufficient to hold Q6 cut off, especially as Q8 is also cut off by the comparator. So Q2 is allowed to conduct, the output voltage rises until first D2, and then Q5, cut off and the output voltage is restored to comparator control.

The ± 38V output is taken through wired-in fuses F1 and F2. These merely protect the PCB tracking in the event of an output short-circuit. The output voltages are protected from reverse polarity by D1 and D2 on the Mother assembly.

4.16.3.5 ± 38V Supply Failure

(Circuit Diagram 430450 Page 7.9-4)

The ± 38V output voltage is monitored in the Power Amplifier assembly. For a description of the monitor refer to Section 4.12, para 4.12.8.

4. 16. 3. 6. ± 400v Common -2 Supply

Refer to section 12, para 4. 12. 7. 2.

SECTION 5

SERVICING AND INTERNAL ADJUSTMENTS

5.1 INTRODUCTION

This section provides procedures for maintenance operations which require removal of covers or partial dismantling. The operations fall into three categories, as described in Table 5.1 below.

Category A Routine Servicing	Servicing Required	Time Interval	Procedure Section 5	Calibration Required	Calibration Procedure
	Clean the Air Intake Filter	1 year (or less in adverse conditions)	5.2	No	—
	Change the Lithium Battery (non-volatile calibration memory)	5 years	5.3	(a) Full pre-cal THEN (b) Full routine recalibration	Section 1.4 Section 1.2
Category B	Internal calibration adjustments	—	—	NONE REQUIRED	

				Calibration required	
Category C	PCB Assembly	Adjustments	Procedure Section 5	Pre-cal (Sect.1.4)	Routine (Section 1.2)
Adjustment following replacement of PCBs (see notes opposite).	Terminal	Capacitive Load Test	5.5	—	Full
	Digital	—	—	Full	Full
	Reference Divider	—	—	Full	Full
	Output Control	Capacitive Load Test	5.5	—	Full
	Sine Source	—	—	—	Full
	AC	Capacitive Load Test Sense Amp zeros	5.5 5.9	— —	Full
	Current	Quiescent Current Compliance	5.6 5.7	— —	All I ranges
	Power Amp	± 120V	5.4	—	—
	Mother	Common-mode null	5.8	—	—
	Out-guard PSU	Common-mode null	5.8	—	—
	Heatsinks +ve & −ve PSU & I	± 120V Quiescent Current	5.4 5.6	— —	— All I ranges
	Transformer HF or LF Mains (Line)	— Common-mode null	— 5.8	— —	1kV Range —

TABLE 5.1 CATEGORIES OF SERVICING AND INTERNAL ADJUSTMENTS

WARNING

HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTION

After any maintenance operations which include removal of top or bottom ground assembly, carry out the Full Self-Test sequence (Section 2.3) before returning to normal use.

CAUTION

The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

5.1.1 GENERAL

(a) Set Power OFF before attempting to dismantle the instrument (for dismantling and reassembly instructions consult Section 3).

(b) After servicing ensure that all connections have been made (Section 3, Fig.3.6) and that Top and Bottom shields and covers have been replaced. Leave assembled instrument powered-up for at least 1 hour before carrying out any adjustment.

(c) Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in Table 5.1 must be carried out to ensure correct operation. These adjustments need to be carried out when the assembly is in the user's instrument, in order to account for interaction between assemblies.

WARNING

HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTION

After any maintenance operations which include removal of top or bottom ground assembly, carry out the Full Self-Test sequence (Section 2.3) before returning to normal use.

CAUTION

The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

5.1.1 GENERAL

(a) Set Power OFF before attempting to dismantle the instrument (for dismantling and reassembly instructions consult Section 3).

(b) After servicing ensure that all connections have been made (Section 3, Fig.3.6) and that Top and Bottom shields and covers have been replaced. Leave assembled instrument powered-up for at least 1 hour before carrying out any adjustment.

(c) Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in Table 5.1 must be carried out to ensure correct operation. These adjustments need to be carried out when the assembly is in the user's instrument, in order to account for interaction between assemblies.

5.2 CLEANING THE AIR INTAKE FILTER

DATRON PART NO. 450277-1
(REFER TO SECTION 3.14, FIG.3.8)

5.2.1 Servicing Frequency

The filter should be cleaned at intervals no greater than one year. In dusty conditions the frequency should be increased.

5.2.2 Removal (Fig.3.8)

(a) Remove the four M3 x 10mm pozi-countersunk screws (11) which retain the filter grille (12).

(b) Remove the filter grille and reticulated foam filter.

5.2.3 Cleaning

(a) Wash the foam filter in a dilute solution of household detergent (hand hot). Rinse thoroughly in clean hand-hot water and dry completely, without using excessive heat.

(b) Clean the grille, and the grille holes in the rear panel (Use a vacuum cleaner and soft brush on the rear panel).

5.2.4 Inspection

Examine the foam filter for wear, replacing if links are broken.

5.2.5 Reassembly

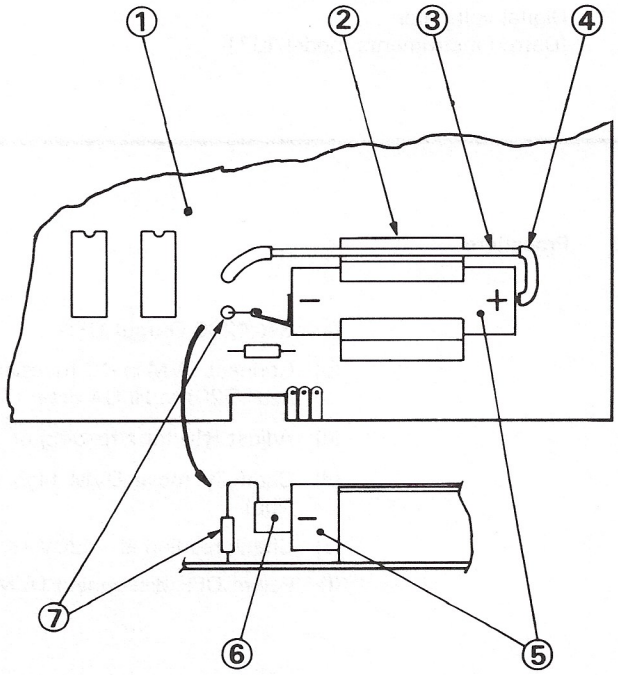
Place the filter in the grille housing and secure the grille to the rear panel using the screws removed in 5.2.2 above.

5.3 LITHIUM BATTERY

(DATRON PART No.920101)

This procedure is to be performed at invervals of 5 years from new.

CAUTION The **full** Pre-cal and Routine Recalibration Procedures (Section 1.4 and 1.2) **must** follow the fitting of a new battery, before the instrument specification can be realized, as calibration data will be corrupted. It is therefore recommended that the battery be replaced immediately prior to a scheduled full recalibration.



1. DIGITAL PCB ASSEMBLY
2. BATTERY CLIP
3. RED WIRE
4. SLEEVE
5. BATTERY
6. NEGATIVE BATTERY TERMINAL WRAPPED AROUND WIRE FROM RESISTOR R60
7. RESISTOR R60

FIG. 5.1 DIGITAL PCB BATTERY REPLACEMENT

5.3.1 Procedure

(a) Ensure that power OFF is selected.

(b) Remove the top cover and top ground/guard assembly
(Section 3 paras. 3.2.1 and 3.4.1).

(c) Remove the digital pcb assembly from the chassis
(Section 3 para. 3.6.1).

CAUTION Do not place the digital pcb on any conducting surface. Do not touch the gold edge connector.

(d) Remove battery as follows (Refer to Fig.5.1).

(1) Push sleeve (4) back along the red wire to expose the solder joint.

(2) Unsolder the red wire (3) from the positive terminal of the battery.

(3) Unsolder the negative terminal of the battery (5) from resistor R60 at the wrap-joint.

(4) Remove battery (5) from battery clip (2).

(e) Fit a new battery, reversing the procedure of step (d).

(f) Refit the digital pcb assembly into the chassis (Section 3 para. 3.6.2).

(g) Refit the top ground/guard assembly into the chassis
(Section 3 para. 3.4.2).

(h) Refit the top cover
(Section 3 para. 3.2.2).

NB The top cover will need to be removed again for precalibration.

5.3.2 Return to Use

Carry out full Pre-calibration then full Routine Calibration in accordance with Section 1.4 and 1.2 respectively.

5.4 ± 120 VOLTS

Adjustment of the 100V/1kV amplifier bias voltages must be carried out after fitting a replacement Power amplifier assembly or Heatsink assembly. The following procedure ensures the drain voltages of Q4 and Q2 are +120V and −120V respectively.

USE EXTREME CARE THROUGHOUT THE FOLLOWING PROCEDURES.

5.4.1 Test Equipment Required

Digital voltmeter
(Datron Instruments model 1071)

5.4.2 Initial Conditions

Remove Top cover.
Remove Top ground/Guard assembly.
Ensure 38V/400V selector is set to 400V.

5.4.3 Procedure

(a) Set 4200 Output OFF.

(b) Connect DVM in DC function, between Lo (⏚2C near Q20) to Hi Q4 drain (Tab).

(c) Adjust R10 for a reading of +120V (±0.5V).

(d) Carefully move DVM high probe to Q2 drain (Tab).

(e) Check reading is −120V (±5V).

(f) Power OFF, disconnect DVM.

5.4.4 Return to Use

Refit Top ground/guard shield and Top cover.

5.5 CAPACITIVE LOAD TEST

(Refer to Layout Drawing 480550)

The 1kv current overload detector, on the Output Control assembly, monitors output current.

After replacing the Output Control assembly, the Terminal assembly, AC assembly or the HF transformers it is necessary to ensure the limit level is set to account for capacitance changes.

The initial value of resistor R33 for the following procedure is 2k ohms. This value is deliberately chosen to give an ERROR OL display with the capacitive load conditions in step (d). If display at step (c) is also ERROR OL then slightly increase value of R33 and restart procedure.

5.5.1 Test Equipment Required

(1) Capacitive Load (150pF ± 3pf, capable of withstanding 2kV).

(2) Digital Voltmeter fitted with AC (Datron Instruments 1071).

5.5.2 Initial Conditions

Top cover removed.
Remove Top ground/guard assembly.
Ensure 38V/400V power supply selector set to 400V.

5.5.3 Procedure

WARNING **THE PROCEDURES INVOLVE THE MEASUREMENT OF LETHAL VOLTAGES. USE EXTREME CARE TO AVOID ELECTRIC SHOCK.**

(a) On the DVM select ACV 1kV range and connect between 4200 Hi and Lo terminals with no load connected.

(b) Select 1kV range on the 4200 and adjust OUTPUT ↑/↓ keys for 750V on the OUTPUT display. Set the frequency to 10kHz and select OUTPUT ON. Adjust OUTPUT ↑/↓ keys for a DVM reading of 750V ± 1V.

(c) Note OUTPUT display reading. Set OUTPUT OFF and disconnect the DVM. Connect the Capacitive Load between the Hi and Lo terminals.

(d) Select 100kHz, OUTPUT ON. Check Mode display for the presence of the ERROR OL message.

(e) On 4200 Select OUTPUT OFF, Power OFF (DO NOT TOUCH RESISTOR R33 WITH POWER ON)

(f) Increase the value of resistor R33 on the Output Control board. Set Power ON and re-establish OUTPUT display reading.

(g) Repeat (d) to (f) until the 4200 will just drive the Capacitive Load at 100kHz, at the output voltage noted in (c), without producing the ERROR OL message.

(h) Finally increase R33 value by the smallest available increment and refit the Output Control assembly in the instrument.

5.5.4 Return to Use

Refit Top ground/guard shield and Top cover.

5.6 CURRENT PCB—QUIESCENT CURRENT ADJUSTMENT

To allow a measurement of quiscent current in the power amplifier stage, its power supply lines are broken and a 0.1ohm resistor inserted in series with each 22V supply line.

The voltage developed across either of these resistors gives a current measurement. The quiescent current is set by adjustment of R23 on the Current assembly.

5.6.1 Test Equipment Required

(1) Digital Voltmeter
(Datron Instruments model 1071)

(2) Two 2.5 watt resistors, 0.10 Ohms, ± 10%, Wire Wound (Welwyn W21 or equivalent)

5.6.2 Initial Conditions

Top cover removed.
Top ground/guard assembly removed.

5.6.3 Procedure

(Refer to Layout Drawing No.480555 and Circuit Diagram No.430555 Page 7.8-1)

(a) Switch the 4200 Power OFF.

(b) Break the 22V supply connections to the Voltage-to-Current converter power stage by removing connector J1 from the In-guard power supply pcb.

(c) Re-make each 22V supply connection from its female pin on the freed J1 connector to its corresponding male pin on the In-guard P.S pcb, using one 0.1 Ohm resistor in series with each supply line (Red and Brown wires).

(d) Connect the digital voltmeter across one of the 0.1 Ohm resistors fitted in (c).

(e) Switch 4200 Power ON.

(f) Ensure 10V range selected with Output OFF.

CAUTION In the following step (g), use a thin insulated screwdriver.

(g) Carefully adjust R23 on I pcb assembly for a digital voltmeter reading of 10mV ± 0.5mV (equivalent to 100mA through a 0.1 Ohm resistor).

(h) Switch 4200 Power OFF.

(i) Disconnect and remove both 0.1 Ohm resistors and the digital voltmeter from J1. Reconnect J1 to the In-guard Power Supply pcb pins.

5.6.4 Return to Use

Refit top ground/guard assembly and Top cover.

5.7 COMPLIANCE ADJUSTMENT

Ensure that the Quiescent Current Adjustment Procedure has been completed (Section 5.6).

In the following procedure a DVM is used to measure output current as a voltage developed across a load resistor. Series resistance is then added to one of the power leads to establish a compliance voltage. The change in current output due to compliance is measured and an adjustment made to bring the instrument within manufacturer's specification.

5.7.1 Test Equipment Required

(1) Digital Multimeter fitted with AC (Datron Instruments model 1081).

(2) Test leads, (each containing a 22.1 Ohm resistor).

(3) One 2.5 watt load resistor of 0.10 Ohms, ± 10%, Wire Wound. (Welwyn W21 or equivalent).

(4) A 1.4 Ohm resistor to introduce compliance voltage.

5.7.2 Initial Conditions

Remove Top cover.
Remove Top ground/guard assembly.

5.7.3 Procedure

(Refer to Layout Drawing 480555 Page 7.8-1)

(a) Connect the 0.1 Ohm load resistor between the 4200 current output terminals (I+ /I−).

(b) **LF Adjustment**

Select ACI, 1A full range output at 500Hz. Select OUTPUT ON.

(c) With the DVM, measure the AC voltage across the load and note the reading. Set OUTPUT OFF.

(d) Introduce the 1.4 Ohm compliance resistor in series with the I+ lead. Set OUTPUT ON. Use the DVM to measure the AC voltage across the load and note the reading.

(e) Remove compliance resistor. If there is a change of reading $\geq 5\mu V$ between (c) and (d) adjust R31 to reduce the reading to $< 5\mu V$. After any adjustment of R31 repeat (c) to (e).

(f) **HF Adjustment**

Complete above procedure, leaving the 4200 as selected (ACI, 1A Full Range), but change frequency to 5kHz.

(g) Set OUTPUT ON. With the DVM measure the AC voltage across the load and note the reading.

(h) Introduce the compliance resistor in series with the I+ lead. Use the DVM to measure AC voltage across load and note reading.

(i) If change of reading in (g) and (h) is $\geq 10\mu V$ adjust R10. If any adjustment is made then remove compliance resistor and repeat (g) to (i).

(j) If an adjustment was made at (i) repeat complete procedure from (b) until no further adjustments are required.

(k) Output OFF, disconnect load resistor.

5.7.4 Return to Use

Replace Top ground/guard assembly and Top cover.

5.8 COMMON MODE NULL ADJUSTMENTS

The procedure ensures that after replacement of Outguard Power Supply, Mains transformer or Mother Assembly, any power supply noise breakthrough on the Lo or Guard terminals is adjusted to a minimum. Resistor R12 on the Outguard Power Supply Assembly (accessible through a hole in the Top earth shield) is adjusted to minimize the voltage between Lo and Ground. R25 on the Mother Assembly (accessible through a hole in the Bottom ground shield) is adjusted to minimize noise between Guard and Ground.

5.8.1 Test Equipment Required

Oscilloscope
(with AC input and sensitivity to 100mV/div).

5.8.2 Initial Conditions

Remove Top and Bottom covers.
Ensure all guard/earth screws are correctly tightened.

5.8.3 Procedure

(a) Set 4200 to AC 10V range with Output OFF.

(b) Ensure that the OUTPUT display is 0.000,00 V with local guard selected.

(c) Connect the oscilloscope AC input between 4200 ⏚ (Ground) and Lo Terminals.

(d) Locate R12 on the Outguard Power Supply pcb through the hole in the Top ground/guard assembly (refer to Layout Drawing No.480561 Page 7.10-1).

(e) Select OUTPUT ON and adjust the oscilloscope controls to obtain the noise waveform.

(f) Without touching the Top ground/guard assembly, adjust R12 for minimum waveform amplitude. This should not exceed 1V peak-to-peak.

(g) Select Remote Guard, transfer the oscilloscope AC input connection from Lo to the Guard terminal, and obtain a noise waveform.

(h) Locate R25 on the Mother pcb assembly through the hole in the Bottom ground/guard assembly (refer to Layout Drawing No.480532 Page 7.16-5).

(i) Without touching the Bottom ground assembly, adjust R25 for minimum waveform amplitude.

(j) Select OUTPUT OFF. Disconnect the oscilloscope.

5.8.4 Return to Use

(a) Refit Top cover.

(b) Refit Bottom cover.

5.9 SENSE AMPLIFIER ZEROS

The sense amplifier, located on the AC assembly, is provided with access holes located in the Top ground/guard shield. In the following procedure the reading and adjustment steps are always taken with the 4200 OUTPUT ON and at one-tenth of the selected Full Range value.

5.9.1 Test Equipment Required

Digital voltmeter
(Datron Instruments model 1071).

5.9.2 Initial Conditions

Remove Top cover only.

5.9.3 Procedure

(a) Connect the DVM Hi to TP5 on the AC Assembly. Connect its Lo to the 4200 Lo terminal. On the DVM select the 10V range with filter in.

(b) On the 4200 select the 100V range and set the frequency to 1kHz. Select OUTPUT ON and adjust R122 on the AC assembly for a DVM reading of less than 200μV.

(c) On the 4200 select the 10V range, OUTPUT ON.

(d) Note the DVM reading.

(e) On the 4200 select the 1V range, OUTPUT ON.

(f) Note the DVM reading.

(g) Adjust R107 on the AC assembly to set both (d) and (f) readings to less than 200μV.

(h) If R107 has been adjusted then repeat procedure from step (a) ensuring that the difference between all ranges is less than 400μV when taking polarity into account.

(i) Disconnect the DVM.

5.9.4 Return to Use

Refit Top cover.

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